Tampere University

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# FAULT DETECTION IN THREE-PHASE INVERTER FED CIRCUIT

## Enhancing the tripping capability of a UPS circuit breaker using wave shape recognition algorithm

Faculty of Information Technology
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# ABSTRACT

Kimotho Immaculate Rebeccah Wambui: Fault detection in a three-phase inverter fed circuit
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Uninterruptible power supplies (UPS) are electrical devices that protect sensitive loads from power line disturbances such as source side overcurrents caused by overvoltage and power surges. The critical load in a double conversion UPS system is supplied from an inverter. When overcurrents occur on the load side of double conversion UPS systems, both the UPS system's inverter and the critical load connected to it stand a high risk of damage. Load side overcurrents due to short circuits, ground faults and motor/transformer start-up are very damaging to power electronic components, electrical equipment and cable connections. There exists circuit breakers on the load side designed to trip when a huge overcurrent occurs, thereby clearing the fault. A circuit breaker is normally sized and installed based on the maximum capacity of the host system and trips when a predetermined overcurrent is recorded within a specific period of time. The UPS system's inverter has a pre-set current limit value to protect insulated-gate bipolar transistors (IGBTs) from damage. During an overcurrent, inverters can supply a fault current whose peak value is limited to the IGBT current limit value. This inverter supplied fault current is not high enough to trip the circuit breaker. After an extended period of overcurrent, UPS internal tripping will be activated and all loads lose power. Operation of the UPS in bypass mode supplies the required fault current but exposes the sensitive load to power line distortions. Therefore, it is desired to always supply the critical load via the inverter.

This study targets to design a detection algorithm for short circuits and ground faults with a detection time faster than the UPS system's internal tripping in order to isolate the faulted area, when the inverter is supplying the critical load. To achieve this, first, a MATLAB model was designed to aid in preliminary studies of fault detection through analysing the system behaviour. Secondly, literature review was conducted and a fault detection method selected with the help of the MATLAB model. Next, laboratory tests on a real UPS system were carried out and compared to the MATLAB results. Lastly, the detection algorithm was designed, implemented and tested on a real double conversion UPS system.

The test results indicate that the implemented detection algorithm successfully detects short circuits and ground faults well within the desired time. It also successfully distinguishes short circuits and ground faults from other sources of overcurrents such as overloading and transformer inrush current. Future development of this study includes additional features such as a fault classification method proposed for implementation to improve the UPS debugging process during maintenance. Moreover, the detection algorithm will also be refined and developed further to activate a circuit that discharges a current pulse to increase the fault current fed to the circuit breaker.

Keywords: fault detection and classification, overcurrent, uninterruptible power supplies, NPC inverter, Simulink, wave shape detection

# PREFACE

This Master of Science thesis was written in association with Eaton Power Quality Oy between March and October 2019.

I thank God Almighty for the gift of life and granting extraordinary opportunities to an ordinary girl and without whom I am nothing.

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Espoo, 15 October 2019

Immaculate Rebeccah Wambui Kimotho

# CONTENTS

# LIST OF SYMBOLS AND ABBREVIATIONS

| | |
|---|---|
| 2L | two level inverter |
| 3L | three level inverter |
| 93PS | Eaton 20 kVA double conversion UPS units |
| A | amperes |
| AC | alternating current |
| AI | artificial intelligence |
| ANN | artificial neural network |
| ATS | automatic transfer switch |
| C | capacitor |
| CB | circuit breaker |
| CPLD | complex programmable logic device |
| CSI | current source inverter |
| CWT | continuous wavelet transform |
| DC | direct current |
| DWT | discrete wavelet transform |
| EMI | electromagnetic interference |
| FL | fuzzy logic |
| FPGA | Field Programmable Gate Arrays |
| FUL | fault under load |
| HSF | hard switching fault |
| IGBT | insulated-gate bipolar transistor |
| kVA | kilovolt-amps |
| L | inductor |
| MRA | multiresolution analysis |
| NPC | neutral point clamped |
| OCP | overcurrent protection |
| PWM | pulse width modulation |
| SPWM | sinusoidal pulse width modulation |
| STFT | short time Fourier transform |
| UPS | uninterruptible power supply |
| VSI | voltage source inverter |

| | |
|---|---|
| $3PH\_g$ | three-phase to ground fault flag |
| $\frac{d\varphi}{dt}$ | instantaneous rate of change of flux with respect to time |
| $\frac{dv}{dt}$ | instantaneous rate of change of voltage with respect to time |
| $f_{carrier}$ | frequency of carrier signal |
| $f_{ref}$ | frequency of reference signal |
| $i_{a,b,c}(t)$ | instantaneous inverter output currents phase values |
| $I_{a,b,c}$ | input current fuzzy universe of discourse |
| $I_{a_m}, I_{b_m}, I_{c_m}$ | phase A, B and C transformer inrush currents |
| $Lgsc$ | single line to ground fuzzy universe of discourse |
| $LLsc$ | double line fuzzy universe of discourse |
| $LLgsc$ | double line to ground fuzzy universe of discourse |
| $3Lgsc$ | three-phase to ground fuzzy universe of discourse |
| $m_a$ | amplitude modulation index |
| $m_f$ | frequency modulation index |
| $ms$ | milliseconds |
| $N$ | inverter neutral point |

| | |
|---|---|
| $PhA\_g, PhB\_g, PhC\_g$ | line to ground fault flags for phases A, B and C |
| $PhA\_L, PhB\_L, PhC\_L$ | line fault flags for phases A, B and C |
| $PHA\_short$ | detection algorithm flag for fault in phase A |
| $PHB\_short$ | detection algorithm flag for fault in phase B |
| $PHC\_short$ | detection algorithm flag for fault in phase C |
| $S$ | number of samples |
| $S_{a(1,2,3,4)}$ | Inverter switches in phase A |
| $S_{b(1,2,3,4)}$ | Inverter switches in phase B |
| $S_{c(1,2,3,4)}$ | Inverter switches in phase C |
| $short\_A$ | signal indicating short or ground fault detected in phase A |
| $short\_B$ | signal indicating short or ground fault detected in phase B |
| $short\_C$ | signal indicating short or ground fault detected in phase C |
| $u_{a,b,c}(t)$ | instantaneous inverter output voltage phase values |
| $v_{(a,b,c)}$ | voltage potential in phase a, b and c of transformer primary windings |
| $V_{a,b,c}$ | input voltage fuzzy universe of discourse |
| $V_{aN}$ , $V_{bN}$, $V_{cN}$ | phase output voltages with respect to DC link midpoint |
| $V_{aref}$, $V_{bref}$, $V_{cref}$ | pulse width modulation reference signals of a three-phase inverter |
| $v^*$ | sinusoidal pulse width modulator reference signal |
| $V_{in}$ | inverter input voltage from DC link |
| $V_{in(+)}$, $V_{in(-)}$ | positive and negative DC link voltage potentials |
| $\frac{+V_{dc}}{2}$ / $V_{c1}$ | positive half of the DC link voltage potential |
| $\frac{-V_{dc}}{2}$ / $V_{c2}$ | negative half of the DC link voltage potential |
| $v_{cr1}$ | sinusoidal pulse width modulator triangular carrier signal 1 |
| $v_{cr2}$ | sinusoidal pulse width modulator triangular carrier signal 2 |
| $\chi_E$ | classical set theory characteristic function |
| $\psi_{a,b}(t)$ | wavelet function |
| $\mu_{\tilde{A}}$ | fuzzy membership function |

# 1. INTRODUCTION

Uninterruptible power supply (UPS) systems play a crucial role in providing conditioned and continuous power to critical loads. Power conditioning refers to providing safe and reliable power in the presence of various grid power line disturbances such as overvoltage, undervoltage, sag, surge, spike, frequency variation, outage, noise and harmonic distortion [1]. The rapid growth of information technology and its applications in many sectors has seen UPS systems playing a key role in system integration. System integration is the ability of the UPS system to communicate over a network in order to monitor sensitive loads. In addition, the UPS system should prepare the loads for a safe shutdown in extreme cases such as extended power outages or discharged battery energy storage. Therefore, UPS systems protect the critical loads from grid side disturbances and distortions.

The major components of a UPS system are power converters, energy storages, motors and (or) generators. The UPS system presented in this thesis is widely used in data centres. With the widespread use of internet and cloud computing services, vast amounts of storage spaces and accompanying infrastructure are essential. Data centres form the backbone of this infrastructure through their numerous servers along with computing equipment. The growing demand for data centre services is a key indicator that high reliability of the supplied power is a necessity. Interruptions in power supplied to data centres has huge financial implications on service level agreements. For instance, the largest data centres in America have an average of tens of megawatts at peak power consumption [2] . With such a high volume of installed capacity, a power interruption would result in millions of money lost for every second the servers are not in operation. It is vital that the services provided by these data centres remain immune to power quality issues as well as power line disturbances.

UPS systems have gained increased significance due to loads such as data centres that require high reliability and conditioned power regardless of the mains supply. Other examples of critical and sensitive loads requiring UPS systems include medical facilities, life supporting systems, emergency equipment, on-line management systems, industrial processing and telecommunications.

Electric power systems are prone to faults that result in high fault currents which are extremely damaging to the circuit components and insulation. In UPS systems, short circuit, ground and overloading faults are the most common that result into high overcurrents which can be very destructive to both the loads and the UPS systems themselves. Short circuits and ground faults are characterized by a large output current and an accompanying voltage sag due to the low load impedance. The behaviour of currents and voltages during overloading is dependent on the extent of the overload. Faults can occur

in a UPS system on the source side, within the numerous power electronic components in the UPS system or in the load side. The scope of this thesis is limited to detection and classification of faults that occur in the load side; otherwise referred to as ‘downstream’ faults from here on. These faults occur at the UPS system’s inverter output terminals when loaded. The downstream faults considered are short circuits, ground faults, overloading and transformer in-rush currents.

In a loaded three-phase system, downstream faults may involve one or more phases and the ground or may occur between individual phases alone. Currently, the UPS system does not distinguish the specific phase(s) where the fault is occurring and when the internal inverter overcurrent protection trips, it cuts power to all the loads connected. For instance, when the UPS system is online and a downstream short circuit fault occurs between phase A and the ground, if the inverter cannot supply a high enough overcurrent, the load is dropped and all connected loads lose power. A downstream fault in one of the phases of the UPS systems leads to loss of power even to the other ‘healthy’ phases. This implies that a single localized fault in one of the UPS system phases is propagated through the downstream leading to loss of power to all connected loads. Therefore, to increase reliability and stability of the UPS system, it is important to monitor, detect occurrence and identify the type and location of a downstream fault before performing a localized fault isolation. This provides further protection to the system and prevents possible damages from cascaded faults. The aim of this thesis is to explore ways of providing fast and localised overcurrent protection. This means that if phase A has a short circuit, a sufficiently high current should be supplied to the circuit breaker (CB) in phase A, triggering it and leaving phase B and C to continue working normally.

Fast and localized overcurrent protection requires the implementation of a new scheme that can detect the phase where the fault occurs and turn on a trigger circuit to clear the specific CB. This thesis focuses on how to detect a fault occurring downstream as well as proposes an algorithm to classify the type of fault. To achieve these objectives, first, a literature review is conducted to explore the various fault detection and classification methods that exist and their suitability as solutions. MATLAB Simulation models are then developed for the various fault conditions. The voltage and current relationships in the fault conditions are studied and compared to the threshold values required for implementation of the detection algorithm. In addition, a test unit for the UPS under study is used to run similar fault condition tests in the laboratory. The results are then compared with the simulations and the practical thresholds recorded. Based on the laboratory and simulated result comparison, an algorithm is developed to detect conditions. This algorithm is intended to increase the fault current supply capability of the UPS system by activating a trigger circuit. The tripper shoots a high current spike which is used to trip the CB in the identified faulted phase. The developed algorithm is then tested on the 20 kVA double conversion UPS system (code name 93PS) and progressively refined based on the testing results.

This study consists of a literature review, MATLAB simulations, laboratory testing on a commercial UPS system and software development presented chapter-wise. In chapter

2, three UPS systems' topologies are presented and their different operation modes explored. Chapter 3 discusses the implemented inverter architecture. Downstream faults are examined in chapter 4 and the effect of the inverter topology on the fault condition waveforms studied. Background studies on existing detection algorithms are reviewed in chapter 5 and the implemented method presented. The proposed classification algorithm is introduced and discussed in chapter 6, together with a summary of the popular classification methods. Analysis, comparisons of Simulink and laboratory fault condition tests and test results of the implemented algorithm are presented in chapter 7. Chapter 8 finalizes this study with perspectives on whether set goals were achieved satisfactorily.

# 2. UNINTERRUPTIBLE POWER SUPPLIES

There are three broad categories of UPS systems; namely static, rotary and hybrid static/rotary systems. These categories are briefly discussed in sections 2.1, 2.2 and 2.3. The focus of the thesis is on subsection 2.1.1 also known as double conversion UPS system and will be discussed in more detail in chapter 3.

The UPS topologies can be represented in the block diagram of *Figure 2.1* [3].

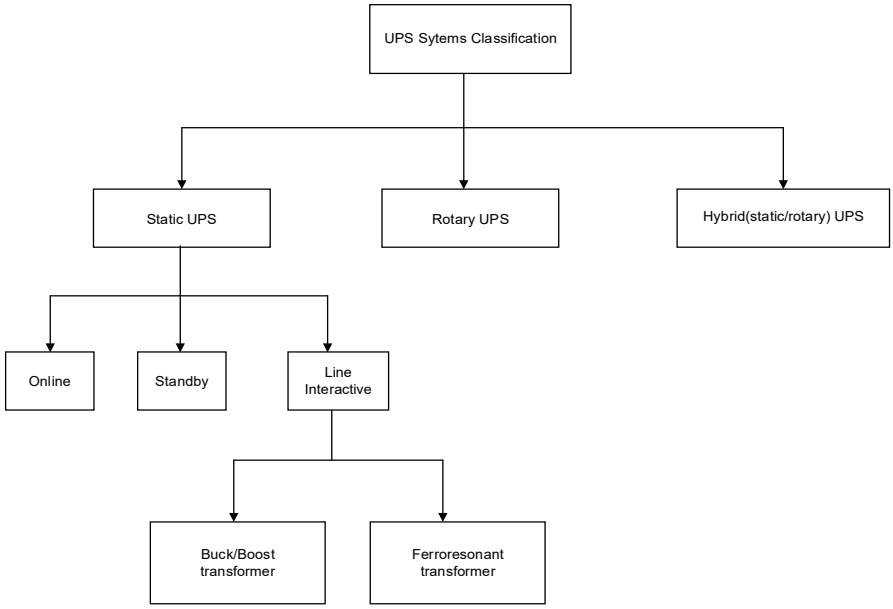



***Figure 2.1** UPS classifications.*

Important factors to consider when selecting a UPS technology includes the electrical properties of the critical load as well as its external operating conditions. Other relevant considerations are reliability, cost and size of the UPS system.

## 2.1 Static UPS systems

A static UPS system uses power electronics to supply power to the critical load instead of a motor or a generator. The main components of a static UPS system are a battery energy storage, an inverter and a converter and/or rectifier. Valve regulated lead acid batteries are the most widely used in UPS systems because they are relatively cheaper than other battery technologies and durable. The converter transforms AC (alternating current) to DC (direct current) to charge the battery and feds it to the inverter. The battery might have an additional converter that steps up or steps down the voltage to the required level. The inverter performs a DC to AC voltage conversion and then feeds the AC voltage to the critical load through a filter.

Due to the wide variety of its applications areas, cost and efficiency, static UPS systems are the most widely used and encountered UPS systems. They can be used for low power applications such as emergency lighting and fire alarms, in medium power medical systems as well as implementation in high power utility applications [4].

Static UPS systems can be implemented in the three topologies listed in *Figure 2.1*, namely, online, standby and line interactive UPS systems. These topologies are briefly discussed in subsections 2.1.1, 2.1.2 and 2.1.3. In Figure 2.2 to Figure 2.13, arrows are used to indicate direction of current flow in the UPS systems.

### 2.1.1 Online UPS systems

This configuration is also referred to as “double conversion UPS” or “inverter preferred UPS” [1], [3], [4] . Block diagram of a typical online UPS during normal operation is shown in *Figure 2.2*. The double conversion UPS system first rectifies incoming AC voltage to DC voltage and feeds this to the DC-AC inverter which provides an AC output to the UPS load. During normal operation, the AC-DC rectifier provides power to charge the battery through the DC-DC converter as well as support the inverter [5] . The flow of current in this operation is as depicted by the arrows in *Figure 2.2*.

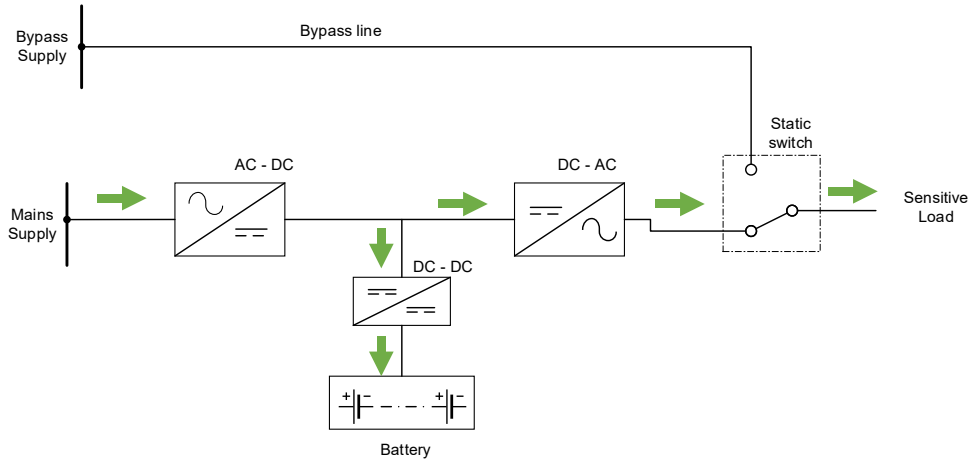



***Figure 2.2*** *Online UPS during normal operation.*

Figure 2.3 depicts the typical response in the event that the mains supply fails or deviates from the input voltage and frequency tolerances. The inverter now operates from battery power to support the AC loads.

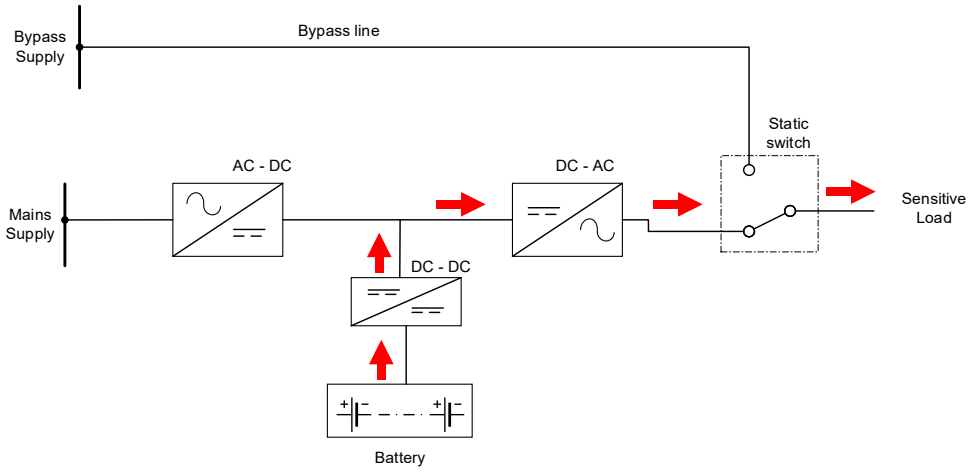



***Figure 2.3*** *Online UPS operation with mains failure.*

It is increasingly common that many online UPS systems have an automatic bypass switch that enhances reliability by providing redundancy of the mains supply, in the event of an overload that the inverter cannot support by itself or a UPS malfunction. The static switch is made of thyristors which are commutated by an external signal to perform switching. The switching speeds of the static switch differ between manufacturers. The Eaton UPS static switch turn on time is $2\ ms$. *Figure 2.4* shows the current path when the bypass switch is in use.

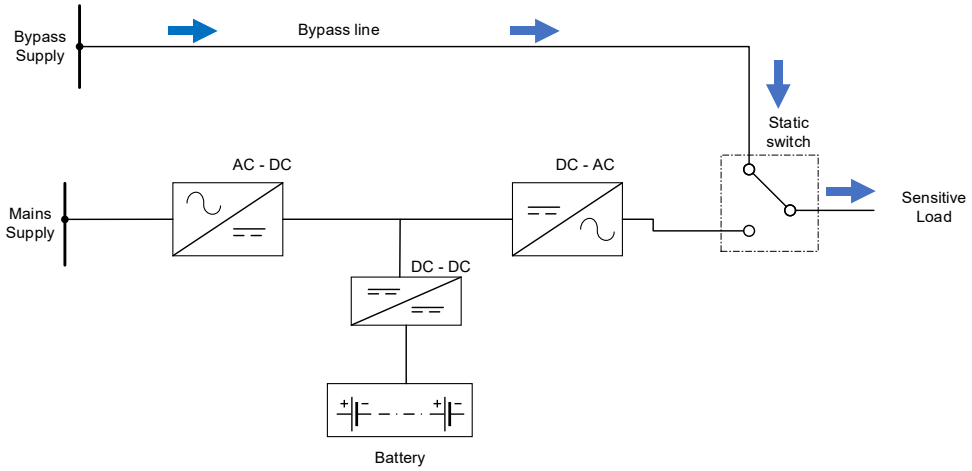



***Figure 2.4*** *Online UPS Bypass switch operational with existing UPS failure.*

## 2.1.2 Standby UPS systems

The standby UPS systems are also referred to as “offline” or “line-preferred UPS” [1], [3]. During normal operation, the critical load is supplied with AC power directly from the mains by the bypass switch as illustrated in *Figure 2.5* without prior power conditioning. This means that the load is subjected to all power disturbances and deviations within the acceptable bypass voltage range that occur. The battery is also charged via the AC-DC rectifier in this operation mode. The AC-DC rectifier in an offline UPS system has a lower power rating compared to one used in an online UPS system as it does not support the load directly. This makes the offline UPS cheaper than an online UPS [6].

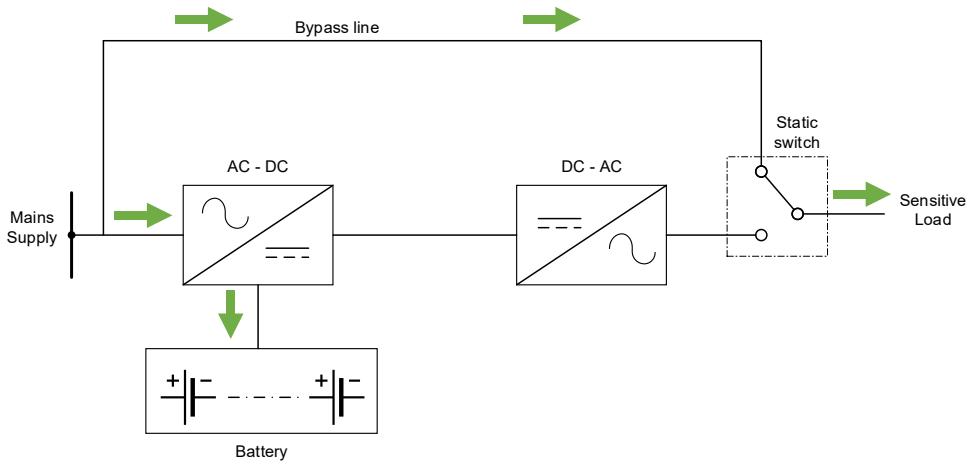



**Figure 2.5** *Offline UPS normal operation.*

In the event of the mains supply is unavailable or disturbances are outside the acceptable pre-set tolerances, the load is transferred from the mains supply to the DC-AC inverter which draws current from the battery storage as illustrated in *Figure 2.6*. The UPS operates in this mode until the mains supply is restored to the desirable limits or the battery is completely discharged and the inverter shuts down through the low voltage cut out.

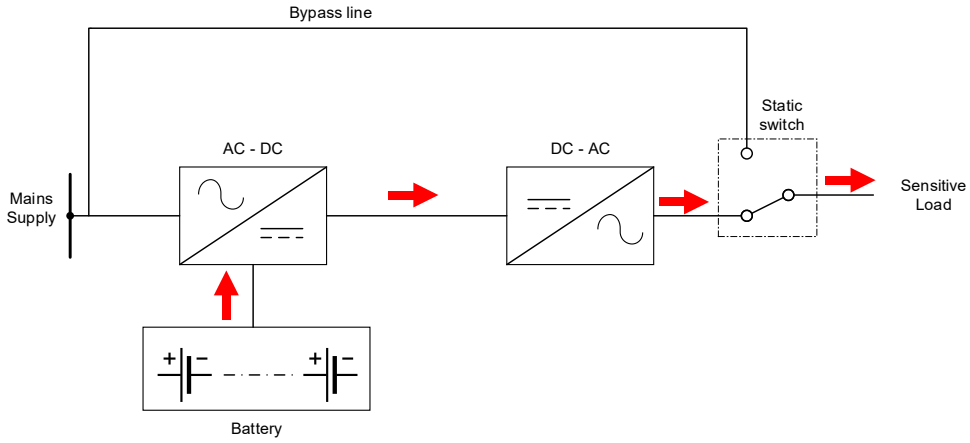



**Figure 2.6** *Offline UPS operating mode with mains supply failure.*

## 2.1.3 Line-interactive UPS systems

A line-interactive UPS system's basic operation is similar to that of the offline UPS system with the exception of the additional circuits observed at the bypass line (see Figure 2.7 below). In normal operation, the AC input is supplied to the load via a filter or transformer. The inverter does not usually support the entire load but is used for instance to buck or boost the line voltage or to smooth out 'notches' in the incoming grid voltage waveform. Therefore, this UPS can interact with the line voltage and thus its name [7].

The two main and most popular line-interactive UPS systems are the buck/boost transformer and the ferro-resonant transformer. *Figure 2.7* and *Figure 2.9* show the normal operation where the load receives power directly via the bypass switch. When the mains power is not within the pre-set tolerances or the power is unavailable, the inverter will supply the load from the battery storage as illustrated in Figure 2.8 and *Figure 2.9*. Due

to the transformers in the bypass line, the load transfer to inverter is less frequent and this significantly reduces the wear on the battery.

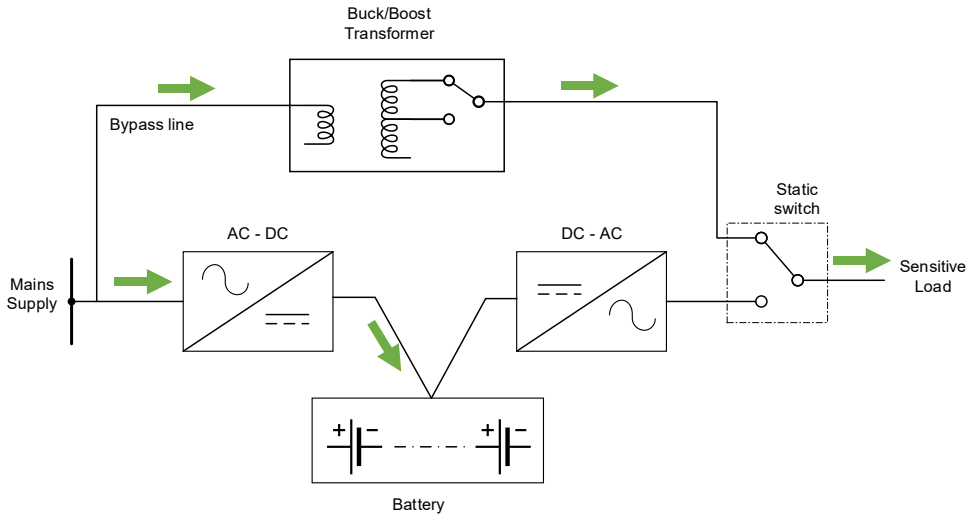



***Figure 2.7*** *Buck/boost transformer UPS in normal operation.*

The transformer secondary windings in the buck/boost transformer of *Figure 2.7* and Figure 2.8 are adjusted by relays to perform mains voltage step-up or step-down, and thus ensuring the desired output voltage limits are maintained [5] . The secondary windings have multiple taps that increase or decrease voltages in steps.

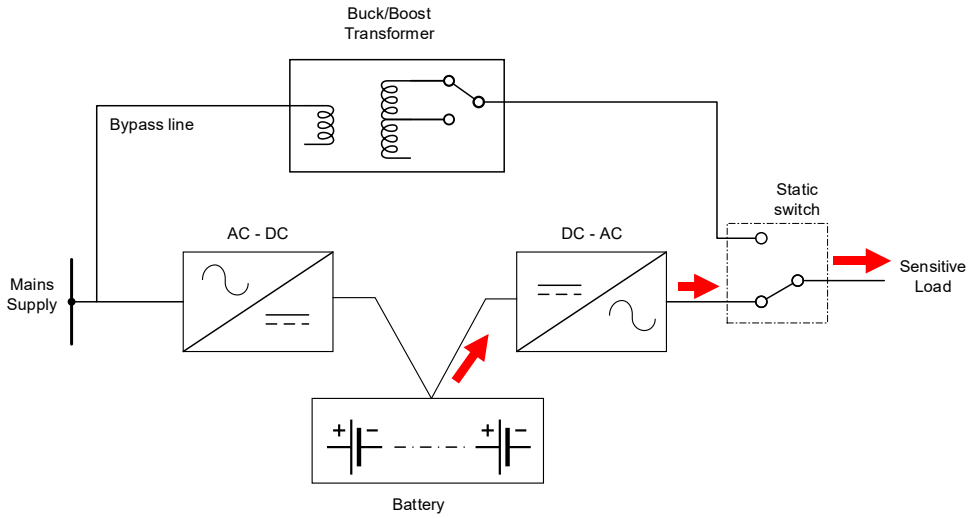



***Figure 2.8*** *Buck/boost transformer UPS operating mode with mains supply failure.*

The ferroresonant line-interactive UPS systems use a bi-directional power converter that charges the battery during normal operation and acts as a power inverter when supporting the load as illustrated in *Figure 2.9* (a) and *Figure 2.9* (b) respectively.

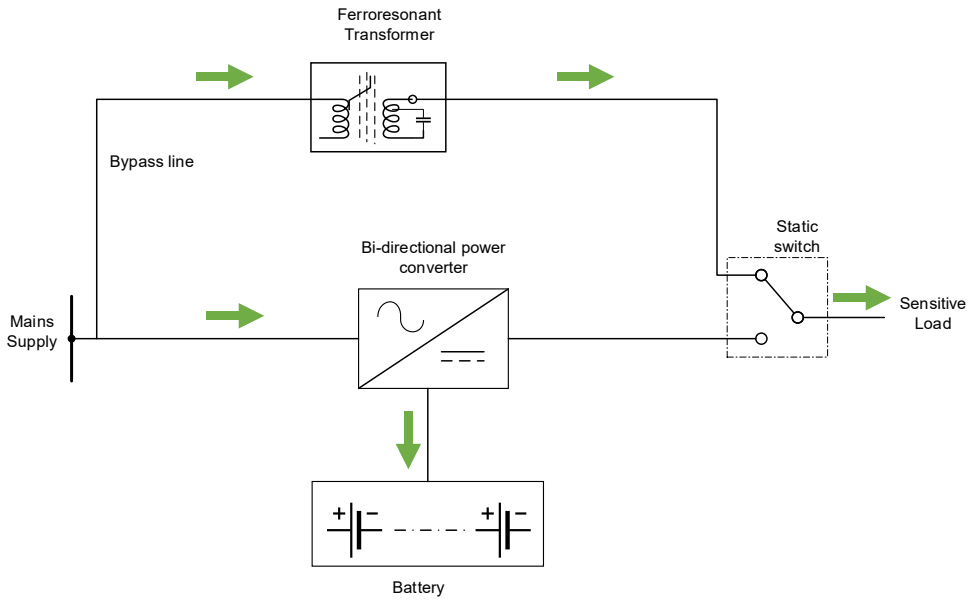



***Figure 2.9*** *(a) Ferroresonant UPS in normal operation mode.*

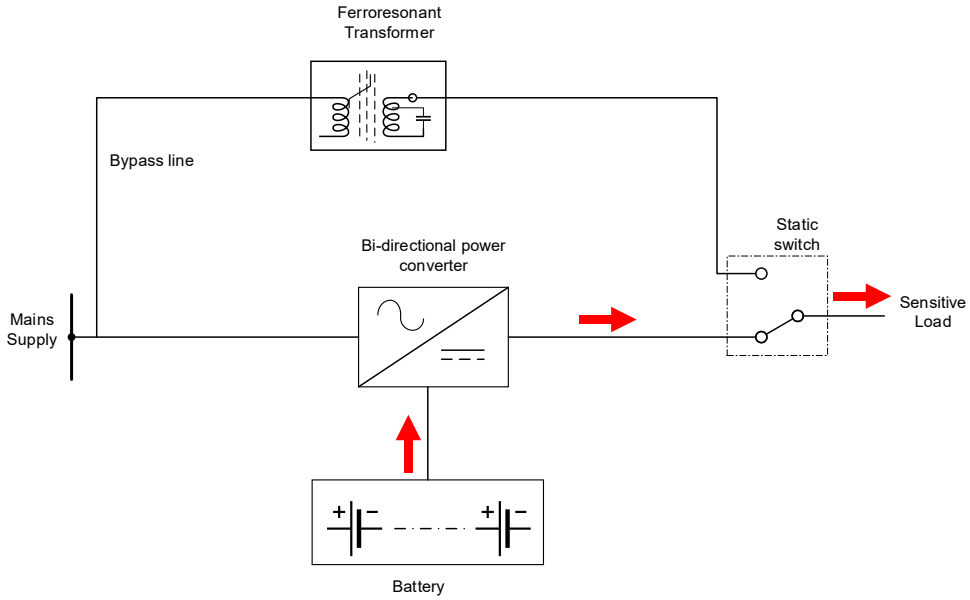



***Figure 2.9*** *(b) Ferroresonant UPS operating mode with mains supply failure.*

## 2.2 Rotary UPS systems

This is the earliest form of the UPS systems having different motor and generator combinations with superior isolation capabilities and an adequate overall performance [8] . They are mainly reserved for industrial applications that require more than 100kVA of protection. These industrial loads are normally large, with non-linear characteristics and a high likelihood of short circuits. Rotary UPS systems have better capabilities to handle these non-ideal loads compared to static UPS systems, but they are more expensive, take up more space and are complex in design.

Figure 2.10 shows a typical rotary UPS system where the electric machines are mechanically coupled. During normal operation depicted by Figure 2.10, the mains supplies power to the load via the automatic transfer switch (ATS) while the synchronous machine performs voltage conditioning via the inductor. Voltage conditioning refers to providing reactive power when needed. The synchronous machine stores kinetic energy to the flywheel by rotating the flywheel mechanically through a connecting shaft.

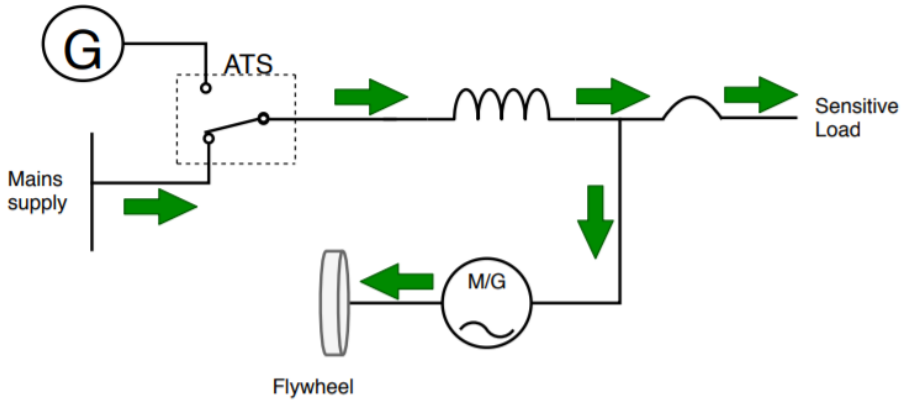



***Figure 2.10*** *Rotary UPS in normal operation mode.*

When the mains supply is inaccessible or operating outside the permissible limits, the rotary UPS system operates in the stored energy mode momentarily until the source side generator starts up. The flywheel discharges its kinetic energy by rotating the synchronous machine, which in turn feeds the sensitive load as shown in *Figure 2.11*.

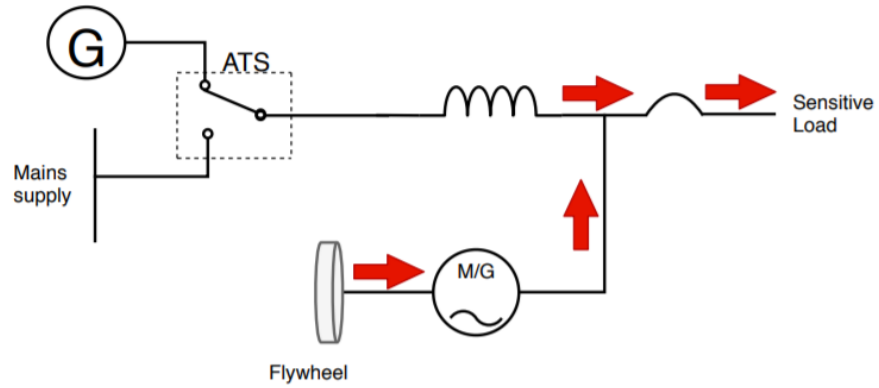



***Figure 2.11*** *Rotary UPS temporary operating mode with mains supply failure.*

*Figure 2.12* shows the operating mode after the source side generator starts up and the ATS connects the sensitive load to the generator supply. The synchronous machine performs voltage conditioning if necessary as well as charges the flywheel.

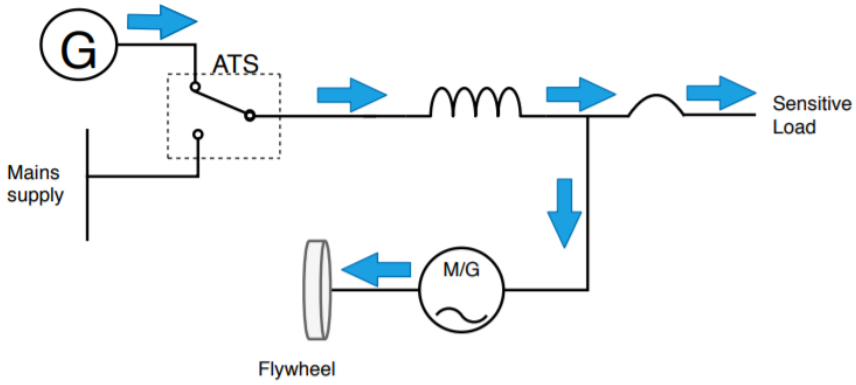



***Figure 2.12*** *Rotary UPS operating mode with UPS failure.*

These UPS systems are bigger in size and weight and require more maintenance compared to static systems [4] .

## 2.3 Hybrid UPS systems

The hybrid UPS system integrates the desirable features of both static and rotary UPS systems. Some of its key features include lower maintenance requirements, high reliability, low output impedance as well as outstanding frequency stability limits [9], [10]. *Figure 2.13* (a) shows the operation of the hybrid UPS system in normal operating, *Figure 2.13* (b) shows operation in energy storage mode while Figure 2.13 (c) depicts operation in UPS failure mode. Hybrid UPS systems are normally installed in high power applications.

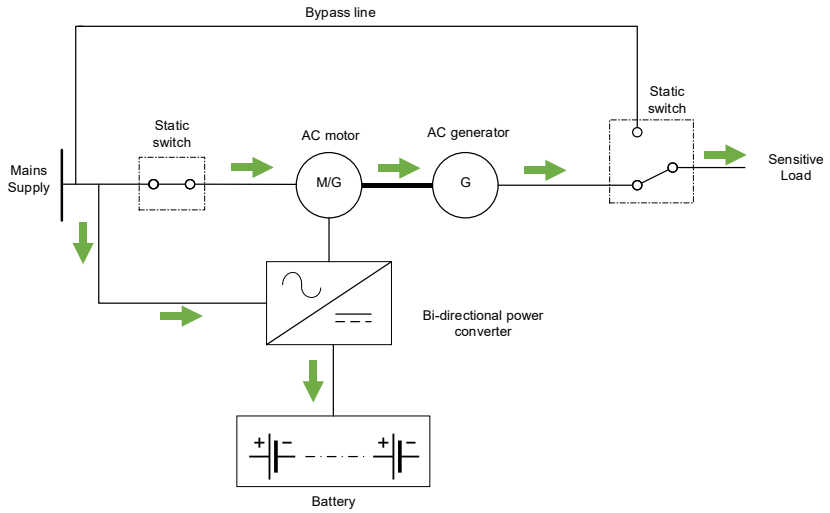



***Figure 2.13 (a)*** *Hybrid UPS in normal operation mode.*

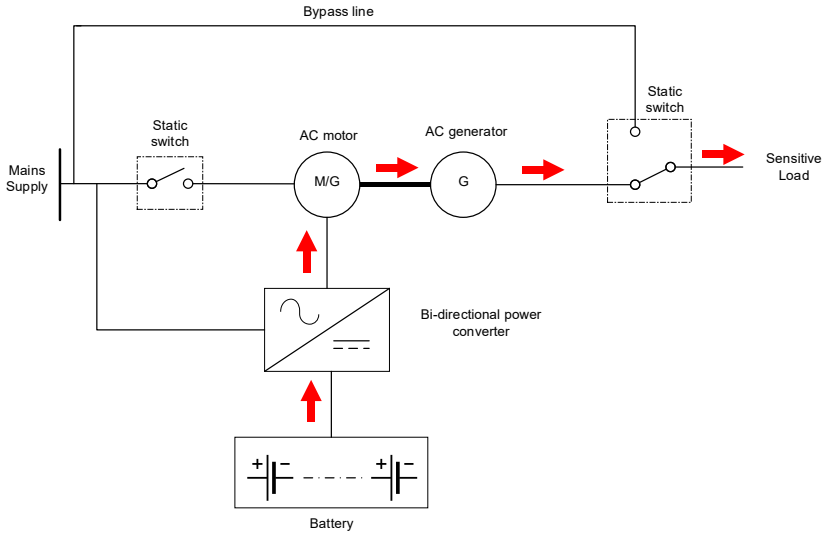



***Figure 2.13 (b)*** *Hybrid UPS operating mode with mains supply failure.*

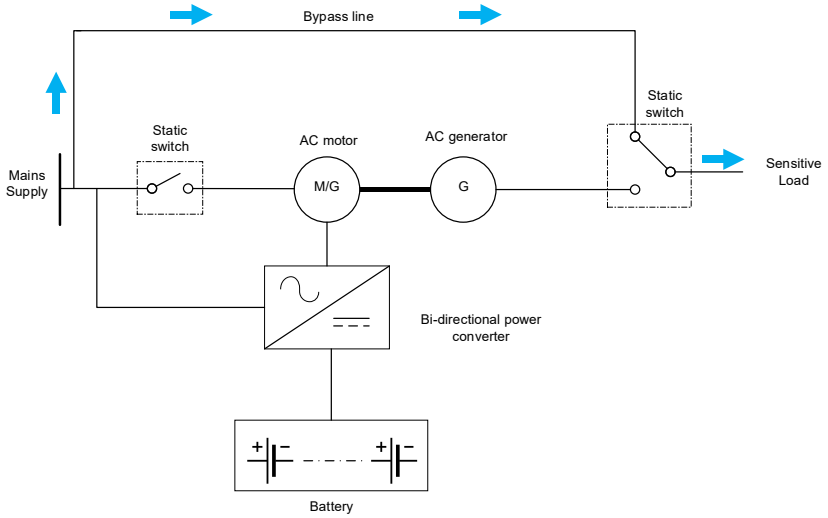



***Figure 2.13 (c)*** *Hybrid UPS operating mode with UPS failure.*

# 3. UPS INVERTER TOPOLOGY

The working of a double conversion UPS system has been discussed in subsection 2.1.1 while Figure 2.2 depicts the general configuration of the system. The inverter fed circuit referred to in this thesis, is a critical load being fed from a double conversion UPS system whose inverter is three-phase, three level(3L) and neutral point clamped (NPC). Three-phase inverters can be two level(2L), 3L or more, also known as multilevel inverters. The number of levels denote the number of voltage potentials to implement the output sinusoidal voltage. For instance, in a 2L three-phase inverter, the possible voltage potentials are $V_{in(+)}$ and $V_{in(-)}$ while a 3L three-phase inverter has $V_{in(+)}$, 0 and $V_{in(-)}$. Multilevel inverters are an inventive strategy for connecting serial switches and have several advantageous features that make them suitable for a wide range of applications.

One of the multilevel inverter desirable features that have made the 3L inverter a good choice for UPS is the fact that for the same DC link voltage, the required switch voltage rating for the 3L inverter is half that of the 2L inverter [11] . This is because a 2L inverter has two switches in every leg as demonstrated in Figure 3.1 while a 3L inverter has four switches in each leg as shown in Figure 3.3. The decrease in the switch voltage rating gives multilevel inverter topologies a significant advantage in that they reduce the voltage stress across the semiconductor switches. Decreasing the voltage stress on switches leads to a corresponding decrease in $\frac{dv}{dt}$ and consequently, a reduction in electromagnetic interference (EMI).

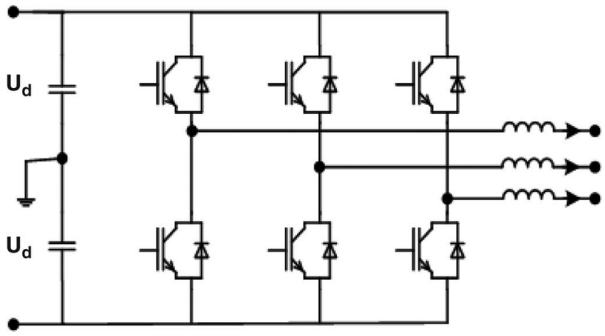



***Figure 3.1*** *Three-phase three-wire 2L inverter topology. Source: Adapted from [12] .*

In addition, the output voltage harmonic content is reduced in multilevel topologies due to availability of more switching states. A cost saving feature of multilevel inverters is that the passive components required in both the AC and DC sides are smaller and lighter compared to the components in lower-level inverter topologies, such as 2L, for the same switching frequency [13] .

A three-phase inverter can be a three-wire or four-wire topology. Figure 3.3 is a three-wire topology while Figure 3.2 shows a four-wire topology. Three-wire inverters are common in applications where the load is balanced while the four-wire topology is used to provide a neutral connection. However, the four-wire topology requires control of the

voltage balance between the split capacitors unlike a three-wire topology. A three-phase 3L NPC inverter can be implemented in both three and four-wire system applications, without further modifications, due to the existing DC neutral point between the split capacitors. In addition, a three-phase 3L inverter is cheaper and easier to control compared to higher level inverters [11].

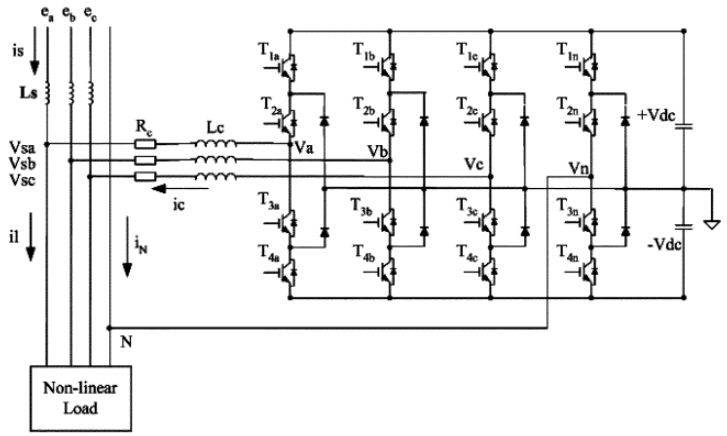



***Figure 3.2*** *Three-phase four-wire 3L inverter topology. Source: Adapted from [11].*

Inverters can be voltage source inverter (VSI), current source inverter (CSI) or Z-source VSI depending on the inverter properties. A VSI inverter has a stiff DC voltage at the source which implies a very small to negligible DC source impedance. The DC source can be from battery storage or a preceding output voltage controlled DC-DC or AC-DC converter. In the case where the DC source impedance is significantly higher, the supply has a stiff current source and the inverter is a CSI. The most common three-phase inverter is the VSI which is the topology used in the UPS under study in this thesis. VSI topology is also used in renewable energy applications where it behaves as a CSI. The Z-source VSI has buck-boost properties and its source can either be a voltage or current source [14].

The NPC inverter, however, has some disadvantages as well. For instance, additional clamping diodes need to be included as illustrated in Figure 3.3 and these additional components take up extra space. Moreover, it has a total of twenty seven switching states and therefore its pulse width modulation (PWM) switching pattern is complicated. In addition, the NPC is used in medium and high voltage UPS applications; Consequently, switching losses are a relevant issue due to increase in the number of switches. Furthermore, the neutral point deviating from its point of balance is an inherent issue that has been widely explored [15]. Despite these disadvantages, the total efficiency of the 3L inverter is higher compared to the 2L inverter because of its smaller output filter.

Figure 3.3 shows the configuration of the 3L three-phase NPC inverter that directly feeds the load in the double conversion UPS systems. The inverter isolates the load into a ‘subsystem’ of what is referred to as the UPS downstream. The load faults will hence be simulated and analysed as a circuit fed from an inverter. The DC link capacitors are charged by the rectifier shown in Figure 2.2.

In the power circuit of Figure 3.3, midway between capacitors C1 and C2 is the neutral point (N) which provides a potential of zero volts with respect to the source. C1 is connected between the positive rail and the neutral point and it maintains a voltage of $V_{c1}$ ($\frac{+V_{dc}}{2}$), while C2 is connected between the negative rail and the neutral point maintaining a voltage value of $V_{c2}$ ($\frac{-V_{dc}}{2}$). The inverter switching stage has been implemented using IGBTs and clamping diodes that connect N to the midpoint between the two upper and two lower IGBT switches per leg. The LC and EMI filters are used to eliminate harmonics for the sensitive load to be connected.

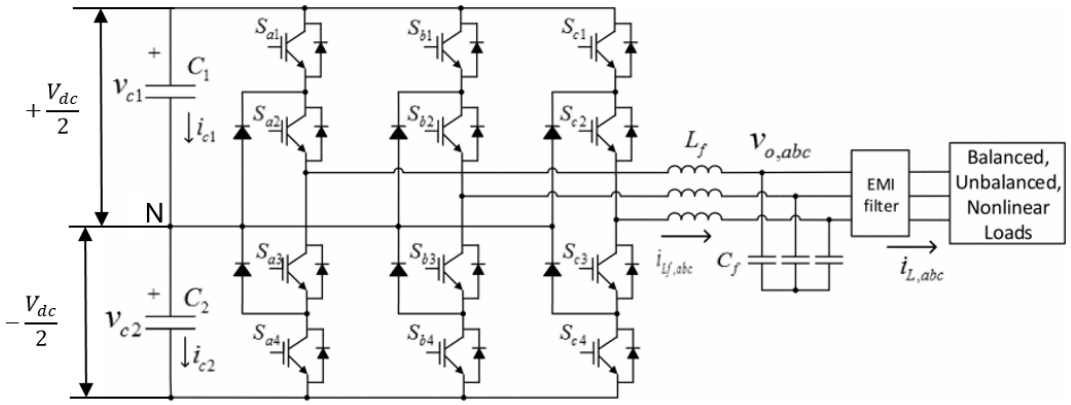



**Figure 3.3** *Three-phase three-wire 3L inverter topology. Source: Adapted from* [16] .

An IGBT is a voltage controlled semiconductor device with very high current handling capabilities (greater than 500A) and a high blocking voltage (600V – 6.2 kV) and a low switching frequency (maximum of 30kHz) compared to MOSFETS, much higher than thyristors which were used in older UPS systems [17] . These are desirable properties for implementation in UPS systems as an electronic switching device. IGBTs cannot conduct in the reverse direction hence, a freewheeling diode is placed in parallel with each IGBT as illustrated in Figure 3.3 IGBTs in VSI get damaged under short circuit conditions and it is important to ensure they are not subjected to high currents [18] .

## 3.1 Basic operation principle

Each inverter leg of the three-phase inverter outputs three different states ($\frac{+V_{dc}}{2}$, 0 and $\frac{-V_{dc}}{2}$). Where $V_{dc}$ is the total potential difference between the inverter positive and negative voltage rails. The output voltages will be denoted as $V_{aN}$, $V_{bN}$ and $V_{cN}$ for 1st (phase A), 2nd (phase B) and 3rd (phase C) inverter legs respectively. Since the switching principle is the same for each of the inverter legs connected to the three-phases, the switching principle of phase A is first explained.

To avoid short circuiting the IGBTs, the switches are commutated in a pre-determined switching sequence with an additional dead time, to achieve these voltage states. From Figure 3.3, the voltage level $\frac{+V_{dc}}{2}$ is achieved when only switches $S_{a1}$ and $S_{a2}$ are turned

on. When only $S_{a2}$ and $S_{a3}$ are on, $V_{aN}$ is at 0V. Output voltage $V_{aN}$ is $\frac{-V_{dc}}{2}$ when only switches $S_{a3}$ and $S_{a4}$ are turned on. It is notable that only one switch is commutated when transitioning from one voltage state to another, thereby, minimizing switching losses [19]. The switching states of phase A are summarised in Table 1.

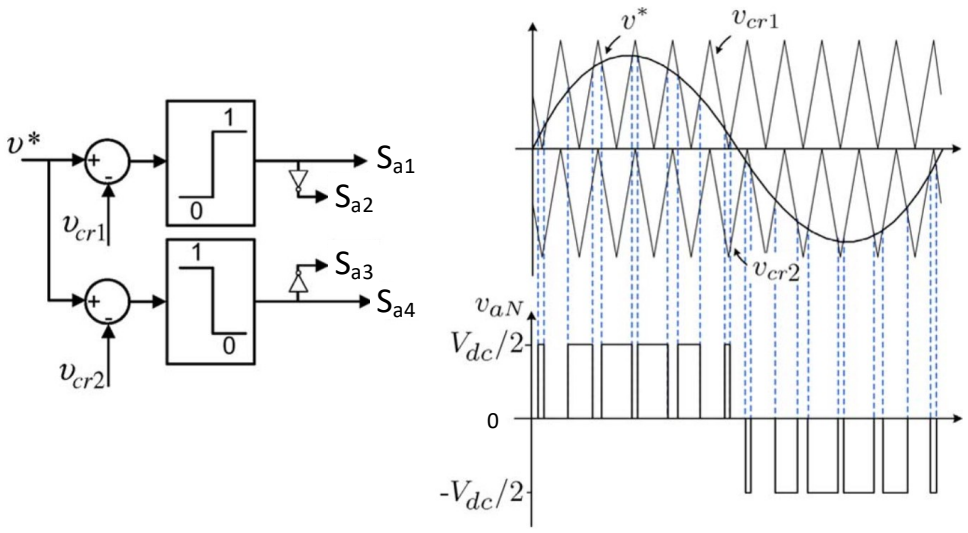
***Table 1.*** *3 phase 3L inverter output voltage levels and switching status.*

| **Switching status** | | | | **Output Voltage** | **Active state** |
|---|---|---|---|---|---|
| $S_{a1}$ | $S_{a2}$ | $S_{a3}$ | $S_{a4}$ | $V_{aN}$ | $S_a$ |
| 1 | 1 | 0 | 0 | $\frac{+V_{dc}}{2}$ | + |
| 0 | 1 | 1 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | $\frac{-V_{dc}}{2}$ | - |

## 3.2 Sinusoidal Pulse Width Modulation

Carrier based pulse width modulation, selective harmonic elimination and space vector modulation are the three most popular modulation techniques for NPC inverters [20] . Sinusoidal Pulse width modulation (SPWM) is the modulation technique used to control the output voltage and frequency in this study. In applications with a DC output voltage, a sawtooth waveform modulation signal is used in order to simplify the system. In our case, the output voltage is AC and a modulation signal with a triangular waveform is more suitable to reduce harmonics.

The basic SPWM control scheme generation of phase A is shown in Figure 3.4.




(a) (b)

***Figure 3.4 (a)****carrier based SPWM modulator* ***(b)*** *gate control signal generation. Source: Adapted from [14] .*

The sinusoidal reference voltage $v^*$ in Figure 3.4 (a) is compared with the two triangular carrier signals $v_{cr1}$ and $v_{cr2}$. The gate control signals generated by the modulator are then fed to the switches in the inverter leg to produce the desired voltage level by a complex programmable logic device (CPLD). Phase A output voltage $V_{aN}$ is determined by the logic summarized in Table 2.

***Table 2.*** *SPWM gate control signals logic.*

| **Carrier & reference signals Comparison** | **Switching status** | | | | **Output Voltage** |
|---|---|---|---|---|---|
| | $S_{a1}$ | $S_{a2}$ | $S_{a3}$ | $S_{a4}$ | $V_{aN}$ |
| $v^* > v_{cr1}$ | 1 | 1 | 0 | 0 | $\frac{+V_{dc}}{2}$ |
| $v_{cr2} < v^* < v_{cr1}$ | 0 | 1 | 1 | 0 | 0 |
| $v^* < v_{cr2}$ | 0 | 0 | 1 | 1 | $\frac{-V_{dc}}{2}$ |

The two level-shifted carrier waves in Figure 3.4 (b) are used to produce the three potential levels. Level-shifting is also illustrated in Figure 3.6; it refers to the offsetting of $v_{cr1}$ above the horizontal axis and setting its values between 1 and 0 while $v_{cr2}$ is offset below the same axis acquiring values between 0 and -1.

Starting with all switches turned off, PWM is performed such that, when the amplitude of $v^*$ is greater than both $v_{cr1}$ and $v_{cr2}$, the modulator feeds a gate control signal to the CPLD that turns on $S_{a1}$ and $S_{a2}$. Phase A output voltage $V_{aN}$ is then connected to the positive DC link voltage and the output voltage is $\frac{+V_{dc}}{2}$.

When the amplitude of $v^*$ is less than $v_{cr1}$ but greater than $v_{cr2}$, the CPLD uses the control signal from the modulator to turn off $S_{a1}$, $S_{a2}$ remains on while $S_{a3}$ is turned on. The output voltage is zero since $V_{aN}$ is now connected to $N$.

Finally, during the time when the amplitude of $v^*$ is less than both $v_{cr1}$ and $v_{cr2}$, the gate control signal fed to the CPLD turns off $S_{a2}$, $S_{a3}$ remains on while $S_{a4}$ is turned on. An output voltage of $\frac{-V_{dc}}{2}$ is then registered at the terminals of $V_{aN}$ which is now connected to the negative DC link voltage.

The switching frequency of the inverter is determined by $V_{cr1}$ and $V_{cr2}$ and thus, they have the same frequency. Harmonic frequencies exist at the switching frequency and at multiples of the switching frequencies as well. High frequency components do not propagate significantly in an AC network or the UPS system's sensitive loads. Therefore, higher frequency values of carrier signals may seem advantageous. However, with higher switching frequencies, the IGBTS have more power loses due to the large number of switchings per cycle and thus it is generally maintained at maximum 10 kHz for high power applications. Phase shifting $V_{cr1}$ and $V_{cr2}$ by $180^{\circ}$ reduces the harmonics and the LCL and EMI filters adequately filter out any other harmonics [18].

The fundamental frequency of $V_{aN}$ (50 Hz) and its amplitude is determined by the reference signal ($v^*$ in Figure 3.4(b)) also known as the control signal [14] . The ratio of the frequencies of the carriers to the reference signal is known as the frequency modulation ratio, denoted as $m_f$, can be presented as in equation (1). Where $f_{carrier}$ is the frequency of the carrier signal and $f_{ref}$ is the reference signal's frequency. An even frequency modulation ratio, as calculated below, gives a more symmetric output waveform for a $360^{\circ}$ cycle. A higher frequency modulation ratio is preferred, as discussed above, as it increases the frequency at which harmonic occur.

$$m_f = \frac{f_{carrier}}{f_{ref}} \tag{1}$$

The ratio of the amplitude of the reference signal to the carrier is known as the amplitude modulation index, usually denoted by $m_a$, can be expressed as:

$$m_a = \frac{v_{ref}}{v_{cr}}, \tag{2}$$

where $v_{ref}$ is the peak value of the amplitude for $v^*$ and $v_{cr}$ is the peak amplitude value for $V_{cr1}$ and $V_{cr2}$ as shown in Figure 3.4(b). Depending on the amplitude of the reference and carrier signals, the inverter can operate in three regions. These has been illustrated in Figure 3.5 where linear, overmodulation and square wave regions of operation are shown for an $m_f$ value of 15 in a three-phase inverter.

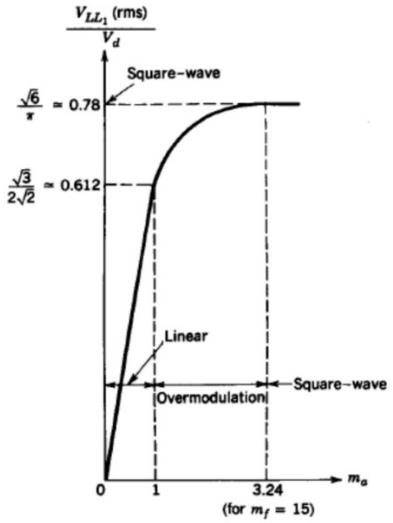



***Figure 3.5*** *Three-phase linear, over- and square-wave modulation. Source: Adapted from [18].*

When $v_{ref}$ and $v_{cr}$ have equal amplitudes, $m_a$ is equal to 1. When the inverter is operating such that $0 < m_a \leq 1$, it is said to be operating in the linear modulation region. When the amplitude of the reference signal is greater than the carrier, $m_a > 1$ and the inverter is working in the overmodulation region. If the amplitude of the reference was to be increased even more such that $m_a \gg 1$, the inverter would operate in the square wave region. The linear modulation region is the normal and desired inverter operation region. When the inverter has downstream short circuit faults connected to ground, it works in the square wave modulation region. This shall be further discussed in chapter 4.

The modulation of phase B and C is identical to the technique of modulating phase A explained above. To achieve modulation of all the three-phases in a 3L inverter, each inverter leg requires its own sinusoidal reference signal. Therefore, the SPWM control scheme in this case has a total of three reference signals ( $V_{aref}, V_{bref}, V_{cref}$) and two triangular carrier waves (carrier 1, carrier 2) as shown in Figure 3.6. The reference waveforms are $120^{\circ}$ phase shifted from each other. They can be expressed as:

$$V_{aref}\,(\omega t) = m_a \sin \omega t \tag{3}$$

$$V_{bref}\,(\omega t) = m_a \sin(\omega t - \tfrac{2\pi}{3}) \tag{4}$$

$$V_{cref}\,(\omega t) = m_a \sin(\omega t + \tfrac{2\pi}{3}) \tag{5}$$

where $m_a$ is the amplitude modulation index and $\omega$ is the angular frequency of the reference signals.

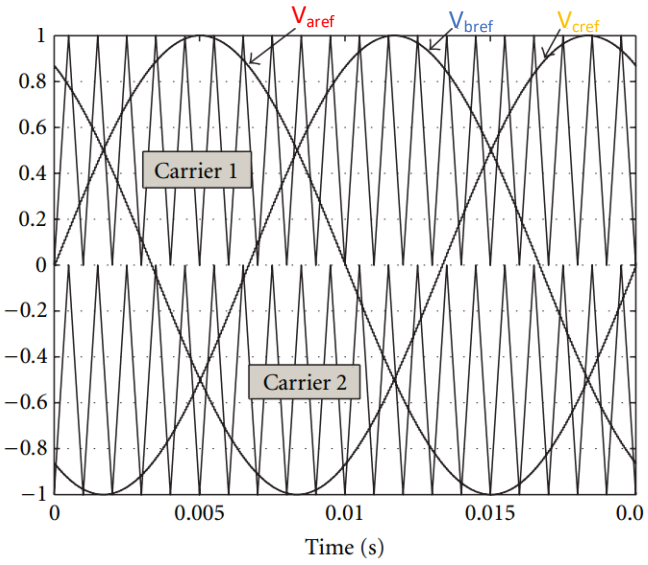



***Figure 3.6*** *Three-phase inverter carrier and reference signals Source: Adapted from [21].*

The amplitude of the fundamental frequency component of output voltages in each of the three-phases can be represented as in in equation (6), when the inverter is in the linear modulation region.

$$v_{ph(a,b,c),fund} = m_a \frac{v_{dc}}{2}, \tag{6}$$

Where $m_a$ is the amplitude modulation index, and $v_{dc}$ is the DC link voltage.

In this region of operation, the output voltage is linearly proportional to the DC side voltage. In case of variations in the DC side voltage, the output voltage can be kept constant through adjusting the amplitude of the reference signals $V_{aref}$, $V_{bref}$ and $V_{cref}$. The maximum output voltage for each of the phases is attained when $m_a = 1$. From equation (6), the fundamental line to line voltage is as expressed in equation (7) [18] .

$$v_{LL(a,b,c),fund} = m_a \frac{\sqrt{3}\, v_{dc}}{2} \tag{7}$$

# 4. OVERCURRENT FAULTS IN UPS INVERTER LOADS

An overcurrent is an excessively high current that is much greater than the nominal or rated current in an electric system. Overcurrents occur from situations such as overloading, short circuits, ground faults and motor/transformer start up. When conductors and equipment subjected to this excessive current, the risk of fire or damage from extreme temperature rise is very high. Therefore, overcurrent protection (OCP) is very important in all power systems. OCP mechanisms are designed to protect users and electric equipment from damage. OCP in power systems has traditionally been implemented through current limiters, CBs, fuses and solid-state power switches. Due to their long-established reliability in OCP, they are widely accepted and adopted protection methods. They have pre-set current limit values that define the safety limits for the electric systems. When this safety limit is surpassed, OCP devices interrupt the overcurrent by creating an open circuit. The OCP scheme in use for the UPS systems under study has been implemented using CBs and fuses. Operation of this OCP scheme will be briefly described.

A CB is a current interrupting device that protects circuits from overcurrents through a mechanical switching action. CBs are categorised in different classes that specify their current and voltage ratings as well as their tripping capability and this information is contained in the manufacturer's datasheet. Tripping capability is determined by the amount of overcurrent required to cause mechanical switching of the CB within a specified period of time. An overcurrent of sufficiently high magnitude is needed in order to trip a CB within a short duration of time. Each CB has a rated current with an accompanying time-current characteristic which determines the current threshold to be reached for tripping to occur. CBs are series connected and should be coordinated to operate in a sequence such that the CB closest to the source of the fault current is triggered first. This provides isolation of the fault area from the rest of the UPS system which then continues to function normally. When a CB trips to isolate the fault origin, the process is referred to as fault clearing.

When a downstream fault resulting in an overcurrent occurs while mains power is available, the UPS switches the load to the bypass connection and the load is directly connected main grid. Operation of the UPS system using bypass connection is known as the bypass operation mode. The bypass is able to supply a high enough current for the CB to clear the fault, which should be below the rated current threshold for the bypass fuse. Connection of the sensitive load to the bypass is not ideal since this exposes the load to any existing power line disturbances.

In the case when the main supply is unavailable, the overcurrent is supplied from the battery for the specified inverter time limit. Operation of a UPS system from battery storage is referred to as stored energy mode. Overcurrent supplied by the UPS inverter is of

lower magnitude compared to the overcurrent supply of the grid via bypass. This is because the inverter's IGBTs would be damaged from overheating if a much higher current than its rated current limit is drawn. To protect the inverter from destruction, the UPS has an internal inverter overcurrent tripper. If the battery supplied overcurrent is not high enough to trip the load CB, the entire UPS system trips via its internal tripper cutting off power to the loads. This is referred to as the UPS 'dropping' the load. This overcurrent protection scheme in use then results into total loss of power to the critical load when the UPS drops the load.

The inverter has a predefined constant current value, known as the current limit, set to protect the UPS system and critical load from overcurrent damage. The inverter current limit value for the UPS under study is $72A$ as can be seen in Figure 4.1. During instances when bypass is unavailable, but the grid supply or battery storage are accessible, the inverter supplies a current limited overcurrent ($72A$). The inverter supplied overcurrent is normally supplied for $300ms$ to protect the IGBTs from irreversible damage. The UPS will then drop the load after $300ms$ in case the load CB does not trip. The downstream circuit breaker generally requires a current higher than $72A$ to clear a fault within a short duration of time.

In ideal operation, the UPS system should not transfer the load to bypass during an overcurrent since this exposes the critical load to power line disturbances. Moreover, the inverter overcurrent tripper should not be activated as this results in complete loss of power to the loads in all phases. Therefore, the UPS system's desirable operation during an overcurrent is to identify and isolate the source of overcurrent while keeping the normal loads operational. The main objective of this study to achieve this desired operation by enhancing the tripping capability of the CB when the load is being supplied from the inverter during an overcurrent. This is accomplished by detecting the short circuit, identifying the phase(s) and isolating faulted phase(s) by tripping the CB. This should be done in less than $300ms$ to prevent the UPS system from dropping the load.

Enhancing the tripping capability of the CB refers to providing a short duration current pulse, that is higher than the inverter current limit ($72A$) to trip the load side CB in less than $300ms$ during a short circuit. This current spike is provided by a tripper circuit. A tripper circuit is basically a capacitor circuit that can be controlled to discharge a sudden current spike in the output current in order to trip a desired CB. The tripper circuit enables fault isolation by triggering the CB to trip when the UPS system is operating in current limit mode during an overcurrent. The tripper circuit is already designed to be used together with the detection algorithm.

The primary focus of this thesis is to formulate an algorithm that can successfully detect overcurrents due short circuit faults and trigger the tripper circuit. In addition to this, it should distinguish overcurrents due to short circuits from those caused by overloads and transformer energisation conditions which should not activate the tripper circuit. In order to develop an algorithm that can selectively trigger from short circuit faults only, it is paramount to study the current and voltage characteristics as a result of short circuits, overloading and transformer inrush current conditions.

In this study, the UPS system is always assumed to be in normal operation, as shown in Figure 2.2. Normal operation means that the critical load is always supplied with AC voltage via the inverter. Therefore, in the laboratory test unit provided, bypass and batteries are not available. Consequently, the operation discussed herein considers that the UPS system does not go into bypass or stored energy modes. Eaton manufactures static UPS systems only; they include online, standby and line interactive UPS devices as depicted in the block diagram of Figure 2.1. Double conversion UPS systems are produced in the Eaton's '9 series' devices, while '3 series' and '5 series' devices are offline and line interactive UPS systems respectively. The 9 series device used in this study is the 93PS model.

The laboratory studies conducted in this thesis are based on a 20 kVA Eaton 93PS UPS device supplied from an AC mains with 400V line to line. The 93PS family of devices exists in two models. The basic 93PS model is a three-phase, three level, double conversion UPS system. The second model known as the '93PS marine model' is similar to the basic model with the addition of an input side and an output side transformer. These UPS systems are designed such that each phase can be used to independently power its own single phase load. For example, the UPS system can successfully support a load running on phase A while phase B and C are unloaded. This means that the UPS system can run unbalanced loads. Additionally, all the three-phases can also be used to run a three-phase load. Generally, separate tests are normally run on the unit to determine its behaviour under unbalanced loads. The tests conditions considered here have been run on balanced resistive loads for simplicity.

In subsections 4.1, 4.2 and 4.3, observations are made based on the current and voltage waveforms behaviour when the UPS system is under short circuit, overload and when experiencing transformer inrush currents. Simulink and laboratory results are used to highlight the observations. MATLAB simulation results of the 93PS 20kVA unit shown in this chapter, were conducted as preliminary studies during literature review. The simulations are compared with the laboratory test results from a real 93PS unit. The oscilloscope voltage and current waveforms, from the laboratory test unit presented in this chapter, are used to demonstrate the rationale of the wave shape detection algorithm and have thus been filtered using the scope's own low pass filter to filter out transients and noise. A more comprehensive description of the results is further presented in chapter 7 along with unfiltered raw voltage and current oscilloscope waveforms and measurements. It is important to highlight that the algorithm developed in this study is based upon laboratory experimental data obtained by deliberately creating overcurrents in the 93PS test unit as well as the MATLAB simulations. The laboratory testing stations are not under any exact controlled external conditions that directly mimic a datacentre. This implies that the laboratory test unit has not been placed in a room where the external conditions such as temperature are monitored and controlled and therefore the impact of external working conditions is outside the scope of this thesis.

## 4.1 Short circuit faults

Short circuit faults also known as shunt faults refer to the introduction of a transmission path between two or more conductive elements forcing the potential difference between these elements to be equal or close to zero [22]. These faults occur intentionally or accidentally. The short circuit faults analysed in this study occur downstream when the UPS is loaded during normal operation. Short circuit faults listed in order of frequency of occurrence include single phase to ground, phase-to-phase, phase-to-phase to ground and three-phase to ground faults.

Some common causes of short circuits in electrical loads include old or damaged wire insulations. Insulation may become damaged due to nail or screw punctures during installation or from small rodents such as rats chewing on the wires and thus exposing the conductors. Wear and tear due to aging wiring can cause deterioration of insulation and eventual shorting. In addition, wire connections can also loosen over time leading to physical contact between neutral and live conductors. Further, electrical loads can also develop internal short circuits due to faults or aging thereby drawing huge overcurrents from the UPS system.

According to the topology of Figure 3.3, the load is always connected to the neutral point on one terminal while the other terminal is either at the positive or negative rail depending on the switching state of PWM. Since the neutral point is at zero potential with regard to the source, it effectively acts as the ‘ground’ terminal and therefore the UPS system is vulnerable to all of the listed short circuit faults. For ease of explanation, the terminal connected to the neutral conductor will be referred to as the neutral conductor and the terminal connected to the bus bars as the live conductor.

Inverter supplied overcurrent waveform shapes are different from the waveform shapes for loads directly connected to the grid. Inverter supplied overcurrent waveforms are square wave in shape while directly grid powered overcurrents are sinusoidal. The inverter current limit is responsible for the square wave shaped waveforms. When a short circuit happens, there is a huge and sudden drop in the load impedance value to a very low value, determined by the impedance of the cable connection to the short circuit. For example, T1 and T2 in Figure 7.2 are short circuited by a short cable of impedance $0.4\Omega$. The $0.4\Omega$ is the load impedance value when a short circuit fault is initiated. Due to this impedance drop, the corresponding output current rises very rapidly to a very large value while the output voltage collapses to a near zero value. The inverter current limit is then imposed onto this sharp increase and decrease of the output current during the positive and negative cycles causing the clipping the peaks to achieve the square wave shaped waveform. The voltage waveform acquires a square wave shape due to the current limit imposed on the output current. This phenomenon should not be confused with the square wave region of operation discussed in subsection 3.2.

In power systems analysis, when short circuits occur in only one or two phases of a three-phase system, they are referred to as unbalanced or asymmetrical faults because they cause the system to lose its balanced state. It follows that a short circuit involving

all the three-phases is said to be a balanced fault. This analysis is not applicable to the considered UPS systems since the phases are taken as independent ‘single phase’ systems. Therefore, the analysis made is not based on symmetrical components or load flow calculations.

### 4.1.1 Single phase to ground fault

This fault occurs when the live conductor and the neutral conductor are connected to the neutral point at the same time. This leads to an immediate immense drop in the load impedance and a very high output current is developed. The output voltage then sags deeply, these conditions are maintained for as long as the short circuit persists until the CB clears the fault.

Figure 4.1 depicts a single phase to ground fault in Phase A simulated in MATLAB’s Simulink platform. The nominal output current value depends in the magnitude of the critical load connected to the UPS system. Phase A output current waveform is a square wave that is limited to the predefined current limit value. The output voltage of phase A sags and is maintained to a value very close to zero and is dependent on the value of output impedance when the short circuit occurs.

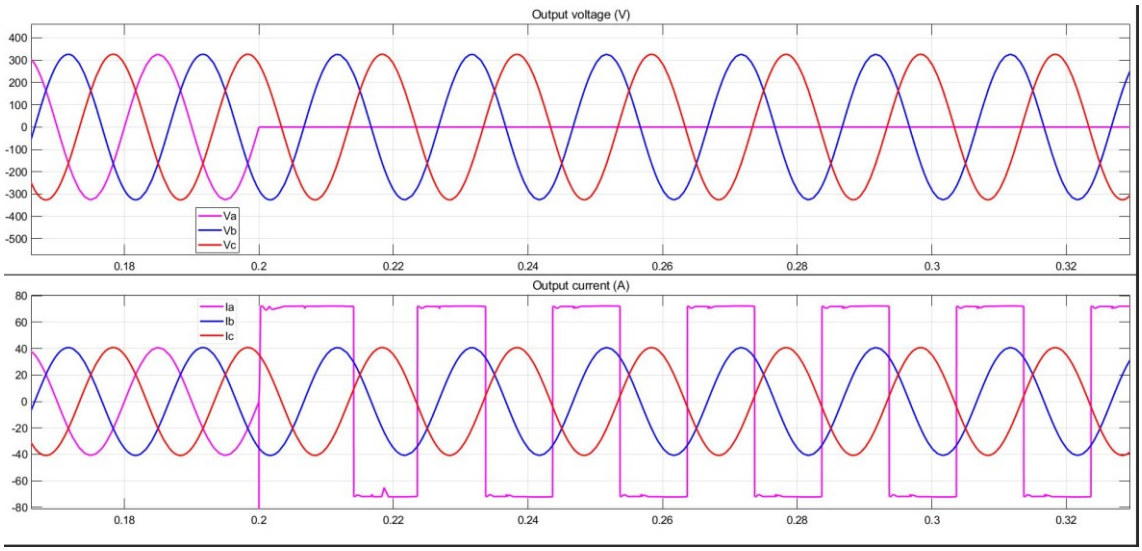



***Figure 4.1*** *Simulated single phase to ground fault in phase A at* $0.2s$.

Figure 4.2 shows the laboratory results with the filtered waveforms having similar behaviour to the simulated results.


***Figure 4.2*** *93PS filtered singlephase to ground fault in phase A.*

### 4.1.2 Phase-to-phase fault

Phase-to-phase fault is also referred to as a double line fault and occurs when the live conductors of any two phases are directly connected to each other. This forces the live conductors to be at equal potential. Figure 4.3 (a), Figure 4.3 (b) and Figure 4.4 illustrate the voltage and current waveform behaviour when this fault occurs in phases A and B.

Figure 4.3 (a) and Figure 4.3 (b) illustrate the MATLAB simulation which differs with the waveforms presented in Figure 4.4. The voltage and current waveforms in the simulation are identical. It is further observed that depending on the resistance of the cable used to connect the two phases when the fault occurred, voltage and current waveforms remained identical while their general shape changed. For example, with higher resistance values, the waveforms are more distorted with a shape similar to Figure 4.3 (b) while low resistance values had waveforms similar to Figure 4.3 (a). The cable resistance used for Figure 4.3 (a) simulation is 0.001Ω while 4Ω was used for Figure 4.3 (b). This difference could be due to the fact that MATLAB simulations are based on ideal conditions as well as components. Another reason maybe that the simulated model differs in design and control methods used in the real system and is therefore not an exact copy thus, the different response.

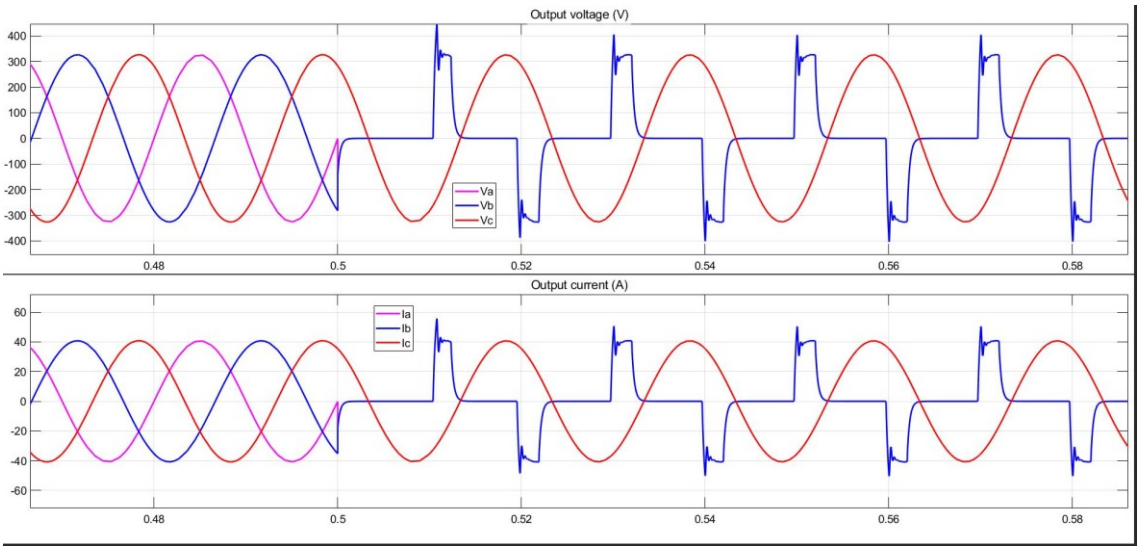



***Figure 4.3 (a)*** *Simulated phase-to-phase fault in phases A and B (0.001Ω) at* $0.5s$.

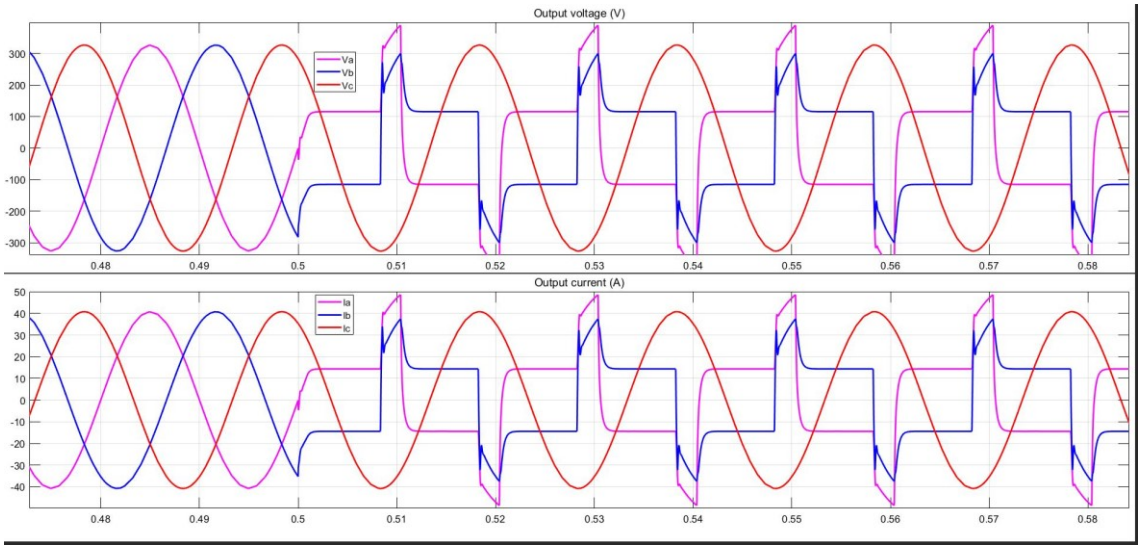



***Figure 4.3 (b)*** *Simulated phase-to-phase fault in phases A and B (4Ω) at* $0.5s$.

The results of Figure 4.4 have been compared with existing Eaton database tests from real 93PS units and are confirmed as the true response of the 93PS unit.

The voltages in the faulted phases (A and B) of Figure 4.4 are in phase with each other and exactly $180°$ out of phase with the 'healthy' phase. The faulted phase voltage waveform has a near zero value before an abrupt rise to a peak value followed by a rapid decay back to the near zero value. This abrupt change in the voltage occurs when the current is transitioning from positive to negative values or vice versa. The current waveform is a square wave waveform and similar to the current limited waveform in the short circuit to ground fault. Phase A current is $180°$ phase shifted from phase B current.

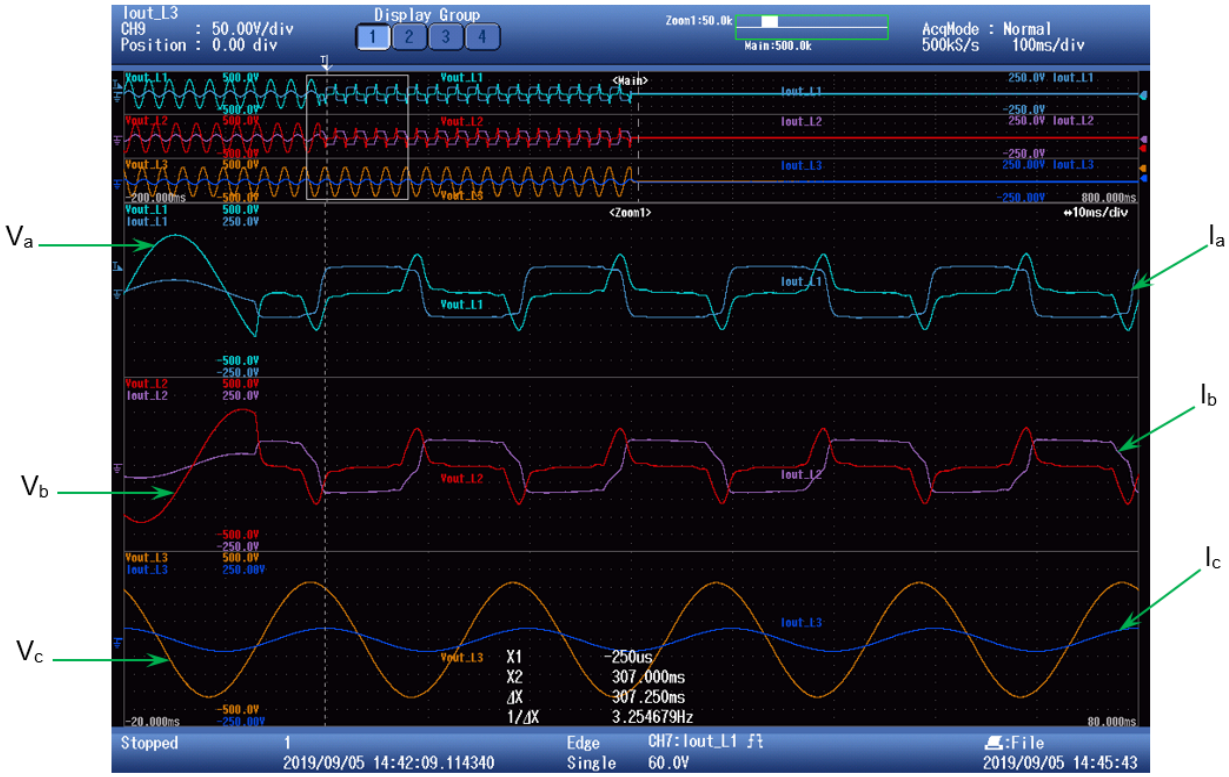



***Figure 4.4*** *93PS filtered phase-to-phase fault in phases A and B.*

### 4.1.3 Phase-to-phase to ground fault

A phase-to-phase to ground fault happens when two phases have their live conductors and neutral conductors all connected to the neutral point at the same time. It is synonymous to having two single phase to ground faults in each of the involved phases at the same time. The output current in the two phases is limited to the current limit value and the waveform is a square wave while the output voltages sag to near zero values.

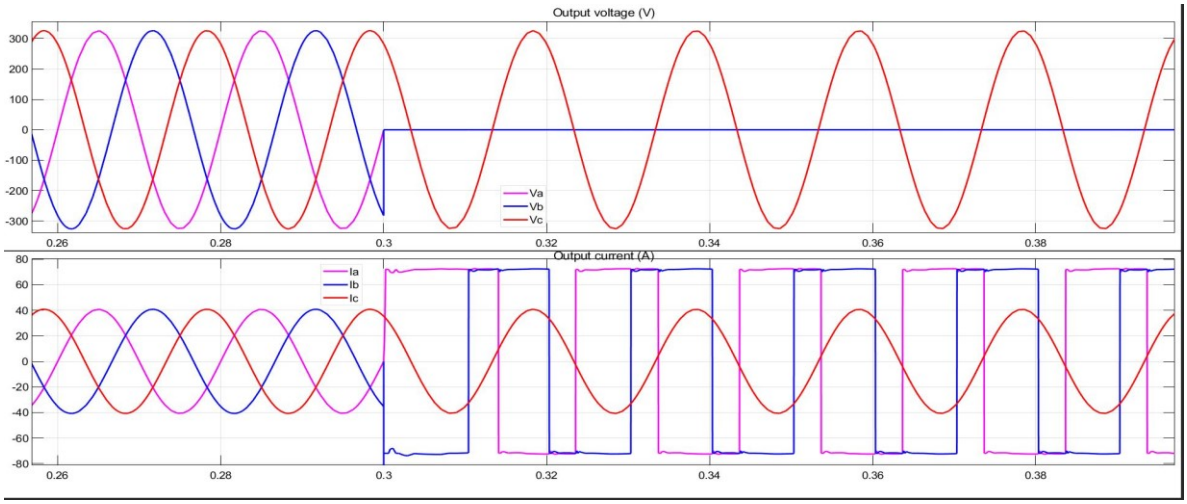



***Figure 4.5 Simulated phase-to-phase to ground fault in phases A and B at*** $0.3s$.

In Figure 4.5, the double phase to ground fault simulated results are presented for phases A and B while Figure 4.6 shows the laboratory experiment waveforms for the fault in similar phases. Waveform results of the laboratory tests and simulations are similar.


***Figure 4.6*** *93PS filtered phase-to-phase to ground fault in phases A and B.*

## 4.1.4 Three-phase to ground fault

When the live and neutral conductors in all phases are all connected to the neutral point at the same, the potential difference is forced to near zero in all the phases. This causes a three-phase to ground fault that is characterized by a huge overcurrent in all phases with an accompanying voltage sag. It is synonymous to having single phase to ground faults in all of the phases. The current is limited to the inverter current limit value while the voltage is maintained at a near zero value with the exact magnitude dependent on the fault impedance. This is illustrated in Figure 4.7 and Figure 4.8.

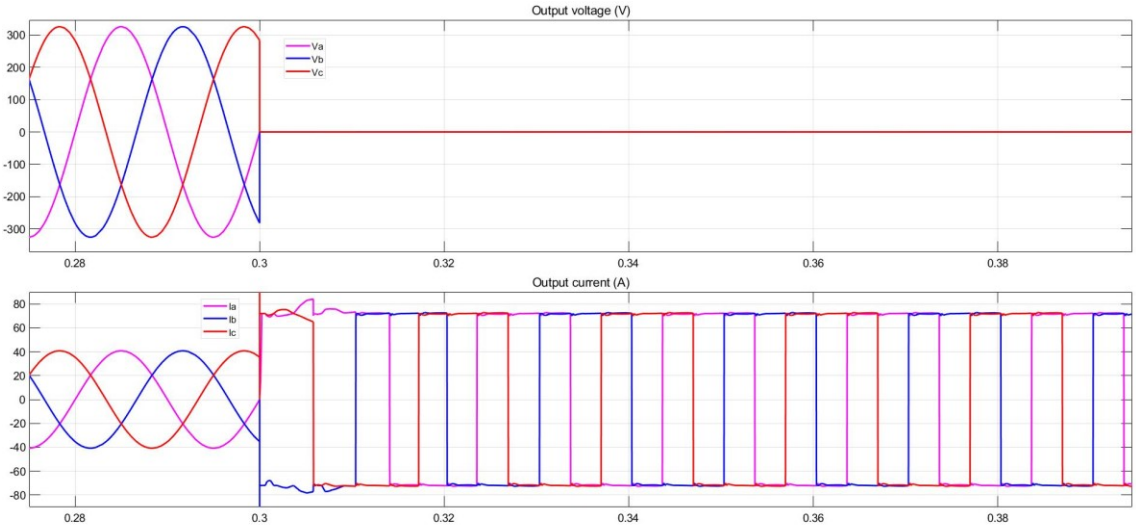



***Figure 4.7*** *Simulated three-phase to ground fault at* $0.3s$.

In Figure 4.8, current in phase A can be observed to have some noise or distortion which is occurs during fault conditions since faults are rarely ideal. Otherwise, the waveform results from simulations are similar to the laboratory test waveforms.


***Figure 4.8*** *93PS filtered three-phase to ground fault.*

## 4.2 Overloading

Overloading can be defined as a ratio of the output current capacity of a UPS system within a defined duration of time to its rated nominal current while maintaining its output voltage within appropriate limits [23] . All UPS systems are rated for a specific nominal

load. If this nominal load condition is exceeded, the UPS systems are designed to support the load for a predefined time which is dependent on the extent of the overload after which the UPS will trip if the overload has not cleared to prevent overheating. This is the overload protection scheme. It is expected that the overload condition is temporary after which the UPS system returns to working within the specified nominal load.

Overload conditions create a bigger load power demand than the rated power. There are different overload capabilities of the UPS depending on the mode of operation, meaning that normal (inverter) mode, battery mode and bypass mode all have unique overcurrent capacities. There are four levels of inverter mode overloading supported by Eaton's UPS systems. They have been graded (from level 1 to level 4) in an increasing level of power demand. Each overload level is calculated as a percentage of the UPS system's rated load value. The levels range from 102% to 150% of rated load. Once the UPS starts working in any of this overload levels, an overload timer will start to run and the UPS system will trip if the overload does not clear within the specified time limit. For instance, a 102% - 110% overload is supported for 10 minutes, 111% – 125% overload for 60 seconds, 126% - 150% overload has a time limit of 10 seconds while overloads above 150% stays online for 300 milliseconds only. Therefore, ideally, the designed algorithm should isolate the faulted phases before 300 milliseconds.

Only level 4 overloading has been considered because the high current it draws is similar to an overcurrent from a short circuit fault. Two three-phase overload cases were tested in the laboratory; $30kW$ and $33kW$ . The voltage and current waveforms of phase A for the $30kW$ overload are shown in Figure 4.9 (a). It can be observed that the system voltage is controlled to the normal UPS system output voltage even with an overload, the output current increases but does not surpass the inverter current limit. This implies that the level four overload is still within the safety limits. Figure 4.9 (b) gives the voltage and current waveforms in all phases for a $33kW$ overload. It can be observed that the current and voltage waveforms are sinusoidal with the peaks shaved to a constant value. At this level of overload, the overcurrent is quite high and the inverter limits this current value shaving off the current peak. This shaved peak current causes the output voltage peak value to have a similar shape.

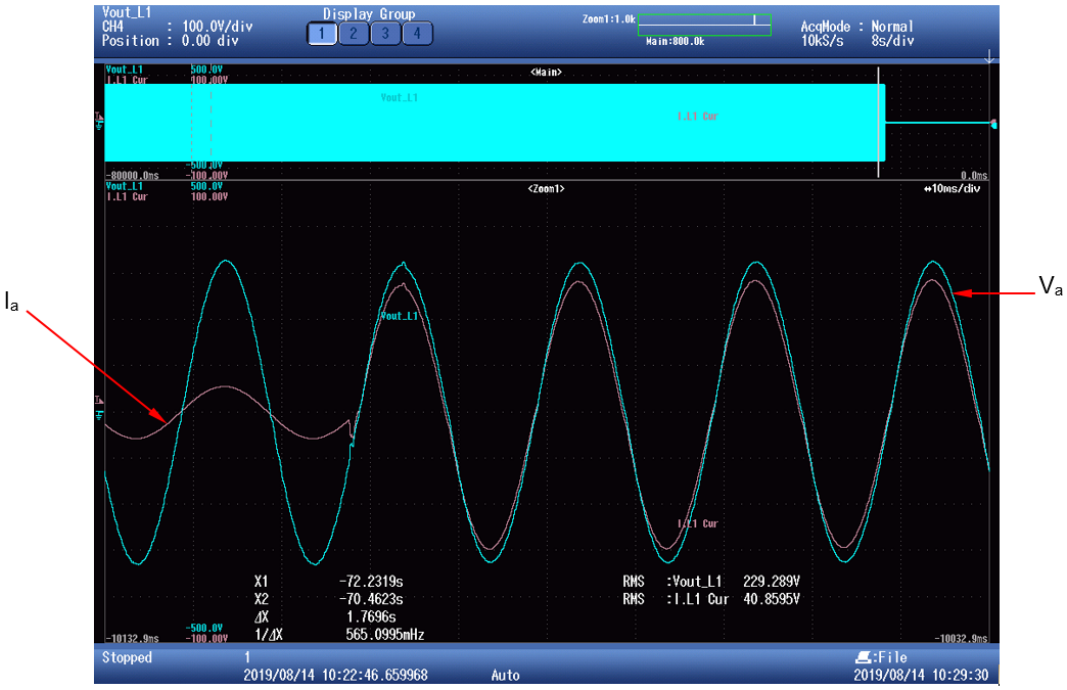



***Figure 4.9 (a)*** *93PS Phase A voltage and current waveforms for 30kW overload.*


***Figure 4.9 (b)*** *93PS voltage and current waveforms for 33kW overload.*

## 4.3 Transformer inrush current

The transformer inrush current is a transient overcurrent condition that occurs during start-up of the marine models. The input side transformer is not analysed as it has no

direct impact on the load side overcurrent. This is because the UPS is loaded after powering up and the input side inrush current happens before the UPS system's loading. The secondary terminals of the output side transformer are connected to the critical load and an output side inrush current is observed when the UPS system goes online for the first time.

Figure 4.10 depicts the 93PS output side transformer inrush currents, $I_{a_m}, I_{b_m}$ and $I_{c_m}$,. It can be noted that for instance, the peak value of $I_{a_m}$ is 91.66A, when the UPS is unloaded. The sizing of marine UPS CBs is done such that an overcurrent occurring for an extended time is required to trip them and therefore, the temporary abrupt transformer inrush current does not cause tripping.


***Figure 4.10*** *93PS output side transformer inrush currents in phases A, B and C.*

The excessively high transient current drawn during energizing a transformer is also known as the transformer magnetization current and can be more than 13 times the nominal load current [25] . This inrush current observed at the transformer primary winding can be described by equation (8),

$$v_{(a,b,c)} = \frac{d\varphi}{dt} \tag{8}$$

where $v_{(a,b,c)}$ is the voltage potential at the primary windings and $\varphi$ instantaneous flux within the transformer core. From equation (8), it can be deduced that the voltage across the transformer primary terminals is directly proportional to the rate of change of flux in the transformer core. When the transformer is energized for the first time, there exists a

residual flux which when added to the instantaneous flux causes the transformer core to saturate. The residual flux is the remaining flux in a transformer core after de-energizing.

*Figure 4.11 (a)* depicts the non-linear relationship between the transformer's magnetic core flux and resultant inrush current. During transformer steady state operation, the operating point on the saturation curve is below the knee point. The knee point refers to the point at which the magnetizing current increases by 50% for every 10% increase in voltage. Beyond the knee point, magnetizing currents increase abruptly even for small voltage increments [25]. At transformer saturation, the operation point shifts upwards above the knee point and consequently, a large inrush current is observed. *Figure 4.11 (b)* illustrates the non-sinusoidal nature of the transformer inrush current as observed in phase A of primary windings of the output side transformer. It is characterized by unidirectional, decaying, sudden current spikes until steady state is achieved.

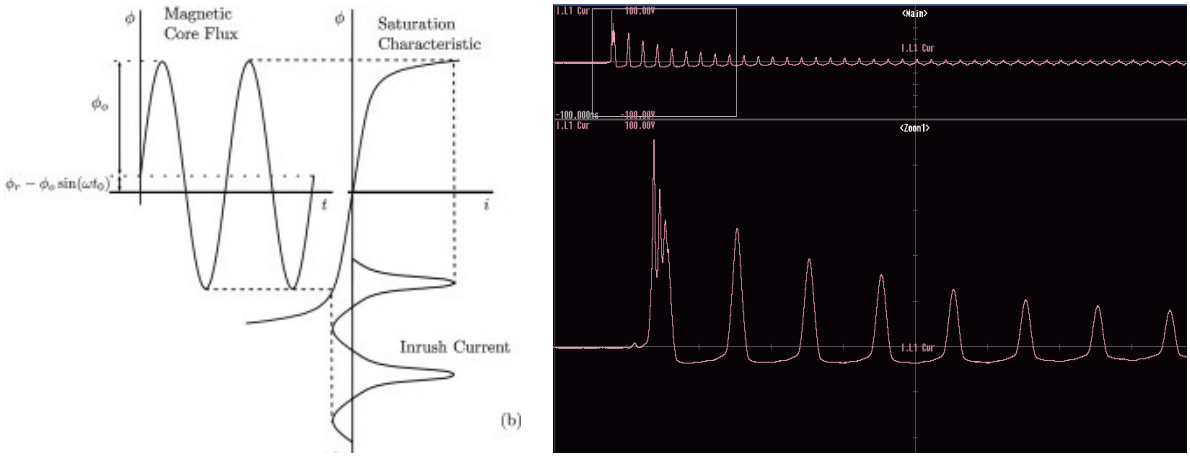



***Figure 4.11 (a)*** *Transformer inrush current production. Source: Adapted from* [24] ***(b)*** *93PS output side transformer inrush current in phase A.*

# 5. FAULT DETECTION METHODS

It is essential to protect power electronic systems from fault conditions through continuous system monitoring, detecting failures, identifying the type of fault and their specific location. This is referred to as fault diagnosis. A fault can be defined as a prolonged unpredicted deviation from the normal system behaviour. Fault diagnosis is the process of establishing the source of a fault based on a set of data from a system with abnormal performance using the fastest and simplest form of analysis. Fault diagnosis mainly constitutes data acquisition, fault detection, location, classification and isolation [26]. The diagnosis function is carried out in the host's microcontroller system.

Fault detection algorithms function differently from fault classification algorithms. Detection algorithms are selected based on factors such as speed of response, inputs available, linearity of the system, harmonics present, processing capability and memory capacity of the host system. The suitability of an algorithm requires close investigation of the host system as well as the desired outcome from the algorithm. Fault classification methods generally require a look up table or dictionary from which the decision making is based. This demands memory allocation depending on the complexity of the algorithm, thus, simpler classification algorithms are preferred. Fault classification methods are predominantly software based and are reviewed in chapter 6.

Several key factors influence the perspective taken for the fault detection methods comprehensively analysed and discussed in this chapter. To begin with, this study views converters on a system level basis and does not focus explicitly on individual power electronic components. This means that the inverter switching components are viewed collectively as a system with a set of inputs and outputs. Secondly, it is vital in UPS systems to keep the inverter on even during short circuits. Therefore, the protection methods should not result in inverter turn off. Another aspect considered was the already designed tripper circuit briefly described in chapter 4. This further set the scope of the study in that, the detection method selected should actuate this tripper circuit. In addition, the fault detection method should operate such that identification of faulty phase(s) is achievable. This is because, it is desirable to perform localized isolation of the phase(s) where the fault has occurred and keep the other phase(s) operating normally.

Isolation of the faulted phases should be performed by the tripper circuit. The tripper circuit is essentially a two capacitor circuit with the capability to provide a very high current spike within a very short period of activation. One capacitor provides a current spike during the positive half cycle while another provides the current spike during the negative half cycle of the output current. Each of these capacitors is connected to a charging thyristor that charges it to the peak value of the output voltage by natural commutation. Natural commutation refers to self-commutation of a thyristor connected to an AC supply as zero crossing happens when the AC supply transitions from positive peak to negative peak and vice versa. The capacitors are then discharged to give the current spike by forced commutation of discharge thyristors from an external pulse source driven by the

developed algorithm. The tripper circuit will be treated as a black box and as such, detailed wiring diagrams are not presented.

System level fault detection algorithms are methods that identify faults in the load side and other parts of a power electronic system other than individual power electronic components [27]. Limited research exists on system level fault detection methods for power electronic converters. This is because switching semiconductors have been determined to be the most frequently prone to irreversible failure and hence, they form the central research focus area for fault detection methods in power electronics [24] - [28]. The focus of majority of the fault detection techniques is protection of these switches from short circuit currents to prevent overheating and their eventual destruction. This is referred to as component level fault detection schemes.

Component level short circuit detection schemes for the power electronic switches are based on the time of occurrence of the fault [29]. For example, when a converter short circuit happens before the converter is turned on, it is referred to as a hard switching fault (HSF) also known as short circuit I, while faults that occur when the converter is running are referred to as fault under load (FUL). FUL is further defined as faults that occur during IGBT conduction (short circuit II) and those that occur when the freewheeling diodes are conducting during the converter dead time (short circuit III). Different fault detection methods exist depending on the time of occurrence, IGBT characteristics, regions of operation and IGBT behaviour during the fault conditions. Collector, emitter and gate voltages and currents are normally monitored to generate a control signal for the IGBT gate pulse. Slow gate turn off is normally the target, in order to limit the turn off transients that occur when the gate turn off is done rapidly.

In contrast, system level short circuit detection methods are primarily dependent on their intended purpose as well as the operation characteristics of the host system. The design process maybe based on reasons such as improving the marketing niche of products by improving their efficiency, increasing features provided by the host system, refining existing detection methods and therefore detection algorithms are tailored to fulfil specific objectives. They require signals measured from the host system and then customized to be algorithm and application specific.

Short circuit detection is generally carried out using hardware methods, software algorithms or hybrid detection methods described in sections 5.1, 5.2 and 5.3 respectively. These are the existing widely accepted and researched mainstream methods that were explored but not implemented in this study due to specific drawbacks mentioned in this text. It was important to assess the key features of the behaviour of the 93PS unit before selection of the fault detection method. Therefore, MATLAB simulation were carried out before and during literature review of fault detection methods in order to compare abnormal system behaviour with the attributes of mainstream detection schemes. These comparisons together with factors such complexity of design, input variables present, speed of response and the level of demand on the host system's resources formed the basis of evaluating the suitability of a fault detection algorithm. The selected and implemented fault detection method is presented in section 5.4.

## 5.1 Hardware detection methods

When the current flowing in a circuit exceeds the rated nominal current for electrical components or circuitry wiring, it is referred to as an overcurrent. Short circuits, overloading, transformer and motor start-ups are examples of events that can cause overcurrents. Overcurrents in electrical systems can lead to system malfunctions due to destruction of components and conductors from overheating. Without overcurrent protection, extreme cases of failure can result in hazards such as fires and explosions.

Overcurrent protection devices have been widely used in power systems to perform current interruption thus preventing system damage. Hardware protective devices include CBs, relays, fuses and solid-state power switches. Hardware detection devices biggest disadvantage is time taken between onset of overcurrent and activation of protection device. Devices that have a lower time delay such as non-resettable fuses normally need manual replacement after an overcurrent has occurred and this results to system downtime. Devices with a higher time delay do not need constant replacement. However, the speed of response is determined by the rate of change of current with regard to time. To minimize the delay before a CB opens during a fault, the tripper circuit in this study has been designed to shoot a current spike so that the CB is always opened within the minimum time limit. Another downside of hardware detection methods is that they are not customized for a specific system. If custom made devices were required, the customer needs to contact the manufacturer directly thereby incurring more cost due to low economy of scale.

## 5.2 Software algorithms

This is the most versatile fault detection method because prominent techniques can be adapted for desired functions. Software algorithms are based on two broad detection approaches, numerical and artificial intelligence methods, discussed in subsections 5.2.1 and 5.2.2.

### 5.2.1 Signal analysis methods (numerical methods)

Numerical methods are well-established and researched classical fault detection techniques, where information is extracted from measured signals obtained from the host system. After signal acquisition, data processing is then performed to determine the system behaviour. Deviations from the predetermined rated values are used to signal abnormality and fault occurrence. Typical Signal processing techniques applied for the detection algorithms comprise instantaneous signal magnitudes, mean and maximum values, variable tolerance values, spectral power densities and frequencies and statistical methods [30].

Frequency domain analysis methods are more favourable in signal analysis compared to time domain analysis methods because they are resistant to distortions caused by noise and switching transients. Signal analysis can be done qualitatively or quantitatively. An exact numerical model of the host system is not needed while performing qualitative

signal analysis and therefore it is more tolerant to harmonics, noise and modelling errors but gives less accurate results. Quantitative signal analysis is a precision method that can determine fault magnitude and location. Frequency domain signal analysis methods used for fault detection are mainly Fourier and Wavelet transform methods.

Wavelet transform has gained significant traction in detection algorithms compared to its Fourier transform counterpart. This is because Fourier transform can only provide information about the frequency components available. It is not possible to determine the particular instant of time certain frequency components come into existence in a non-stationary signal using Fourier analysis. In addition, Fourier transform has a very limited cycle range (signal duration) within which comprehensive information can be extracted from a signal. To solve this problem, short time Fourier transform (STFT) is implemented by using a sliding window to perform Fourier series on the target signal. A sliding window is basically a means by which a small portion of the target signal can be extracted by shifting the window over the signal to be analysed. There arises problems with detecting low frequency components in STFT which can be minimized, but not eliminated, by keeping the sliding window's width constant.

Wavelet transform overcomes all the problems inherent with Fourier transform based schemes. It can be used to analyse signals of any duration and establish time of occurrence of particular frequency components. Due to this quantitative nature, the most prevalent signal analysis method is the wavelet transform [31]. Another advantage of the wavelet transform method is its ability discriminate harmonics from non-linear systems with those resulting from system abnormalities. This is especially important because power electronic circuits are characterized by harmonics resulting from switching of the IGBTs through PWM or other control schemes.

Wavelet transform is the use of mathematical functions to decompose a signal into different frequency components. This enables analysis of a signal within finite energy functions of short durations comprising a family of 'wavelets'. The splitting of the mother wavelet (signal) into smaller wavelets is referred to as wavelet transform. The family of wavelets is formed through a process of translation and scaling by a wavelet transform function. The mathematical notation of a wavelet is represented in equation 9, where $b$ is the translation distance and $a$ the scale expansion [32].

$$\psi_{a,b}(t) = |a|^{-0.5}\, \psi\left(\frac{t-b}{a}\right), a < 0 \tag{9}$$

From equation 9, it can be deduced that the wavelet transform is calculated at different translation distances specified by the $b$ parameter, for varied scales of expansion or compression via the $a$ parameter within the total plane of transformation. Continuous wavelet transform (CWT) happens when wavelet transform is done as a smooth and continuous operation while discrete wavelet transform (DWT) is the transformation done when the translation distance and scale expansion are specified as a set of discretized steps.

Wavelet transform is implemented through filters whose design is based on a selected wavelet family. There exists various wavelet families optimized for signals with certain distinct characteristics. Examples of wavelet families for CWT include Paul, Meyer, derivative of Gaussian and Morlet wavelets, while DWT wavelet families include orthogonal wavelets (Haar and Daubechies) and B-spline biorthogonal wavelets. Selecting the right waveform family is very important and hence, the nature and properties of the signal in the host system must be analysed thoroughly. Selection of Unsuitable wavelet families will result in very complicated and problematic designs whose results may be incorrect.

Due to continuous translation and scaling of the wavelets in CWT, its coefficients after calculations generally tend to infinity, with a lot of redundancy. This makes practical application of CWT cumbersome and therefore DWT is normally preferred. Implementing DWT is simple, however designing filters to perform wavelet transform involves a set of complex calculations and further analysis of the result is required. This translates to more resources in terms of microprocessor memory, processor cycles or time.

This fault detection method although very interesting for further research, was not selected due to its resource intensive nature, complicated computations for filter design and the need develop two other separate algorithms. One that controls the tripper circuit by feeding it with the correct output from the wavelet transform and a second that performs fault classification. In addition, research on wavelet transform based algorithms has primarily been carried out at component level (i.e. for HSF and FUL) [33].

### 5.2.2 Artificial intelligence methods

Artificial intelligence (AI) is the design of intelligent systems that can adequately perceive their surroundings and make decisions that maximize their chances of success. This involves an iterative process of learning and tuning parameters towards the desired outcome. AI systems are designed to work autonomously and simulate human intelligence. These methods are very useful in systems with non-linear responses, inexistent mathematical models and where signals are time-varying with unreliable measurements. The main AI based approaches developed for fault detection are artificial neural networks (ANNs) and knowledge based systems [30]. These fault detection methods can also be applied in successfully classifying faults eliminating the need for two different algorithms.

#### A. Artificial Neural Networks

The key defining feature of ANNs that defines their suitability for implementation in fault detection is their pattern recognition capability. Neural networks can be defined as a set of learning algorithms designed to identify patterns. The design of ANNs is inspired by the biological neural network of the human brain. Due to the high complexity and interconnectivity of the human brain cells, the ANN is not identical but a simplification of the human neural network. Therefore, ANNs are approximation models. To imitate the neurons, ANNs are made up of millions of artificial neurons known as nodes where computations are done. Each node can take input data, perform simple operations and compute an output value which is then forwarded to another node via a link. The node output value is referred to as an activation value [30].

Every link connecting two nodes is assigned a weighted value. This weighted value is an integer number that represents the learned knowledge of the system. Depending on the outcome of the system, the ANN adjusts the weight to increase the accuracy of the result.

Figure 5.1 depicts the processing of data at an ANN node. Each node input is weighted and then a sum of these weighted values is computed. This sum is then subjected to an activation function which generates the activated value to be fed to the next node. The activation function basically determines to what extent the node input values affect the output of the entire ANN. Important node inputs are combined to form the activation value while irrelevant node inputs are filtered out [34] .

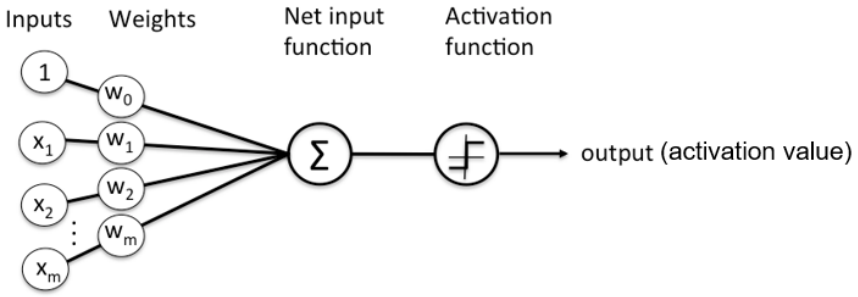



***Figure 5.1*** *Computation at an ANN node. Source: Adapted from [35].*

ANNs are composed of several layers of linked stacked nodes. A layer comprises of several rows of nodes whose activation values are the inputs of the subsequent stacked layer. The general ANN architecture is as represented in Figure 5.2. It is composed of an input, hidden and output layers. The layers interact through links. The architecture design process involves determining the number of layers, number of nodes in each layer, number of hidden layers, activation functions and learning algorithms. Hidden layers represent multiple levels of input value computation and are a measure of the ANN's 'depth'.

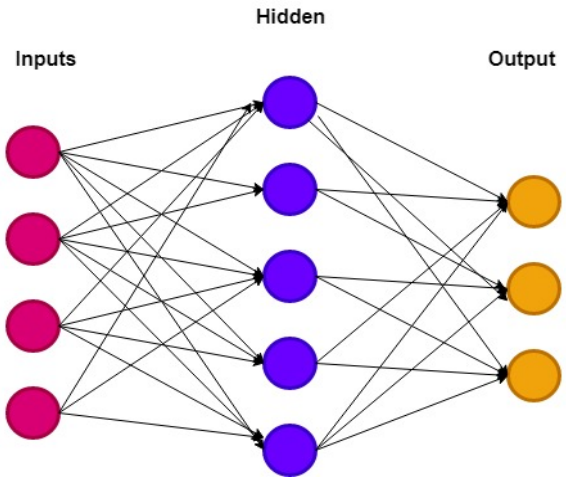



***Figure 5.2*** *The Architecture of an artificial neural network.*

Deep-learning ANNs are characterised by a significant amount of hidden layers. Hidden layers are used to perform complex computations to enhance the pattern recognition performance of an ANN [34] . Although a deeper ANN with more hidden layers and high interconnectivity (many links) is desirable for more intelligent systems, a very powerful processor with superior speeds would be required or the ANN would be very slow. Therefore, there exists a trade-off between depth and interconnectivity at system design.

ANNs learn to recognize patterns through intensive training exercises using strategies such as supervised, unsupervised and reinforcement learning. Supervised learning involves training the ANN using a skilled expert from a particular speciality. The expert trains the system to recognize patterns by feeding it with sample data of already known phenomena. When the ANN is presented with unknown data, it gives some guess results based on the training and then the skilled expert feeds the ANN with the expected results to make comparisons. The learning process is therefore iterative but limited to the competence of the trainer. In unsupervised learning, the ANN is trained to recognize hidden patterns. In this training method, the answers to the data presented is unknown and the ANN trains to recognize patterns through clustering or statistical formulae. The guess results improve over time as the ANN learns. Reinforcement learning refers to training the ANN through observation. There exists known answers that are compared to those of the ANN after its observations of the surroundings. This way, the ANN is trained to recognize patterns based on certain properties of the environment it observes.

ANNs have very good non-linear function approximation capabilities as well as high accuracy especially in well trained systems. Currently, ANNs and machine learning is a widely researched subject full of potential and with an extensive array of application areas. Since it is widely under development, a few challenges exist. For instance, it is currently unclear what is the major factor that determines the intelligence of the ANN. Both the size of the ANN and the interconnectivity of the nodes are crucial, but it remains unclear which of the two should be prioritized in ANN design [36] . Moreover, depending on the learning algorithm selected, the memory needed can be quite huge making ANN very computationally expensive and impractical especially when implemented in real time. In addition, the training process is very tedious. Intensive training to achieve high learning rates requires huge investments in time and trainers. In fact, current research efforts are directed towards developing methods that help determine the neural weights and as such avoid the training step. Due to these drawbacks, ANN is not a feasible solution for this study.

### B. Knowledge based Systems

Knowledge based systems are AI systems whose problem solving abilities depend on a knowledge base and an inference engine. A knowledge base is an organized centralized repository that is used to store data of a particular discipline while an inference engine is the rule making component that deduces information from the knowledge base through logical definitions. Knowledge based systems are normally implemented as expert systems. An expert system is an AI program that solves complex problems in a particular field by emulating the skills, judgement and behaviour of a human expert from knowledge

stored in a database, through inference procedures and a set of if-then rules. The expert system used in fault detection is known as fuzzy logic [30].

Fuzzy Logic (FL) is the only mainstream fault detection method that was explored in depth in this study as a potential fault detection method to be implemented. A model was also created on MATLAB to simulate this method with unsuccessful results. FL and its principles of operation will be briefly introduced, its superior characteristics in fault detection algorithms reviewed, rationale behind its initial consideration as a suitable detection algorithm as well as reasons that made its implementation unsuccessful in this specific application.

FL is defined as a logic used to describe fuzziness. Fuzziness is the attribute of something being vague and lacking in certainty or precision. FL is a suitable fault detection scheme for diagnosis of abnormalities that match with the typical definitions of a fuzzy model. One distinctive attribute of an FL system is that the input to the system has to be fuzzy i.e. the boundaries of the inputs are not exact. The voltage and current values during faults have significant noise and harmonics and therefore the exact input value may be defined as a range of values as opposed to one precise measurement. Moreover, the phase voltage values for short circuit to ground and line to line faults overlap at their boundaries. Another attribute of a fuzzy system model is its ability to handle complex non-linear systems such as the line to line fault voltage waveform whose response is non-linear and difficult to handle. Consequently, an FL based algorithm was viewed as an initial fitting candidate due to these matching properties.

The concept of FL was first introduced by Zadeh in 1965 to model systems whose boundaries are not defined by exact values [37]. It was later implemented by Mamdani in a practical control application after which it gained a lot of recognition [38]. It is based on fuzzy set theory, a subset of classical set theory, from which membership functions are formulated using input values. Membership functions eliminate the need to define an exact threshold value. The input membership functions are subjected to a set of fuzzy rules which yield output membership functions.

Classical set theory can be represented using a characteristic function. Equation 10 defines the characteristic function $\chi_E$ , where $E$ is the subset of $T$ ($E \subseteq T$) such that; $\chi_E : T \rightarrow \{0,1\}$. Member elements of subset $E$ are strictly either 1 or 0. Equation 10 indicates that all elements of $T$ contained in $E$ have a value of 1 while all elements of $T$ not in $E$ have a value of 0.

$$\chi_E(x) = \begin{cases} 1 : x \in E \\ 0 : x \notin E \end{cases}, \tag{10}$$

Fuzzy sets are a simplified extension of classical sets where members are allowed partial membership in the range 0 to 1. Fuzzy member elements can take values such as 0.2 and 0.5. A fuzzy subset $\tilde{A}$ of $R$ can be defined by its membership function $\mu : r \rightarrow [0,1]$. A membership function is the FL equivalent of a characteristic function. Hence, $\mu(r)$ where, $\mu \in \tilde{A}$ , denotes the grade of membership of $r$ in the fuzzy set $\tilde{A}$. $R$ is the universe

of discourse i.e. the range of values that $R$ can assume. A fuzzy set $\tilde{A}$ in the universe of discourse $R$ can then be denoted mathematically by equation 11. Where $\mu_{\tilde{A}}(r)$ is the membership function of $\tilde{A}$ that assumes values in the range of 0 to 1 [37] .

$$\tilde{A} = \{(r, \mu_{\tilde{A}}(r)) | \, r \in \tilde{A}, \; \tilde{A} \subset R\}, \tag{11}$$

Elements of an FL system are illustrated in the fuzzy architecture of Figure 5.3.

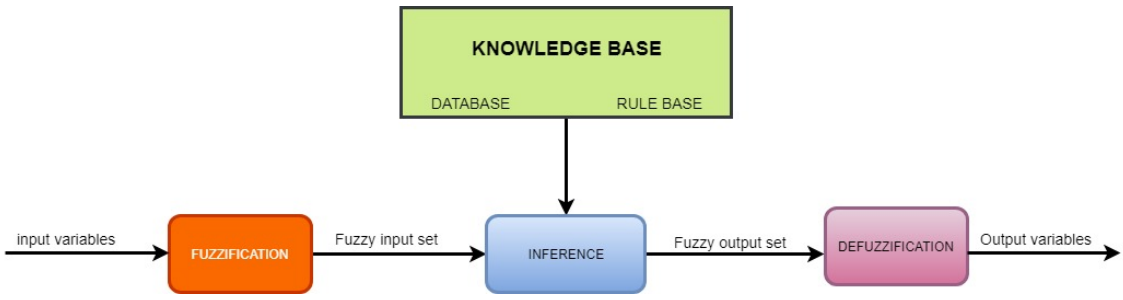



***Figure 5.3*** *Block diagram of a typical fuzzy inference system.*

Fuzzification of the input variables refers to reducing the inputs into linguistic variables. A linguistic variable is a variable whose value is expressed in terms of spoken language. For instance, instead of 10V or 40V, we refer to the voltage as 'low' or 'high'. Inference involves performing operation on fuzzified data based on the knowledge base. The fuzzy rule base is composed of a set of rules that represent an expert's view and understanding of the behaviour of the system under observation. Defuzzification is the process of converting the linguistic data into output variables with numerical value [39]. The fundamental steps followed in formulation of an FL algorithm discussed below with examples from the attempted 93PS FL model. The steps are designed following the process flow of Figure 5.3.

Instantaneous voltage and current values are the desirable input values for fast system response. Instantaneous current and voltage phase values were defined as inputs and output variables are the short circuit condition of the system as shown in equation 12.

$$\begin{aligned} R^n = R^6 = \{I_a, I_b, I_c, V_a, V_b, V_c\} \\ R^m = R^4 = \{Lgsc, LLsc, LLgsc, 3Lgsc\}' \end{aligned} \tag{12}$$

Where $R^*$ is the fuzzy relation, $n$ and $m$ are the number of input and output variables respectively, and $I_{a,b,c}, V_{a,b,c}, Lgsc, LLsc, LLgsc$ and $3Lgsc$ are the universe of discourse. $Lgsc$ is the single line to ground short circuit, $LLsc$ the line to line short circuit, $LLgsc$ the double line to ground short circuit and $3Lgsc$ the three-phase to ground fault.

The input membership functions are defined as:

$$\begin{aligned} I_a &= \{\mu_{I_a}(i_a) | \, i_a \in I_a\} \\ I_b &= \{\mu_{I_b}(i_b) | \, i_b \in I_b\} \\ I_c &= \{\mu_{I_c}(i_c) | \, i_c \in I_c\} \end{aligned} \tag{13}$$

$$V_a = \{\mu_{V_a}(v_a)|\ v_a \in V_a\}$$
$$V_b = \{\mu_V(v_b)|\ v_b \in V_b\} \quad (14)$$
$$V_c = \{\mu_{V_c}(v_c)|\ v_c \in V_c\}$$

The output membership functions are defined as:

$$Lgsc = \{\mu_{Lgsc}(lgsc)|\ lgsc \in Lgsc\}$$
$$LLsc = \{\mu_{LLsc}(llsc)|\ llsc \in LLsc\}$$
$$LLgsc = \{\mu_{LLgsc}(llgsc)|\ llgsc \in LLgsc\} \quad (15)$$
$$3Lgsc = \{\mu_{3Lgsc}(3lgsc)|\ 3lgsc \in 3Lgsc\}$$

Where $i_a, i_b, i_c, v_a, v_b, v_c, lgsc, llsc, llgsc, 3lgsc$ are the elements of the discrete universe of discourse.

The membership functions of equations 13, 14 and 15 are then represented graphically through a clustering process. Examples of graphical representations of membership functions include triangular, trapezoidal, Gaussian, sigmoidal and s-shape functions [40]. The graphical membership function is a curve that determines how the mathematical values of the defined input and output functions are defined in the 0 to 1 range. Figure 5.4 illustrates the membership functions that can be used to mode the input and output of the fuzzy model.

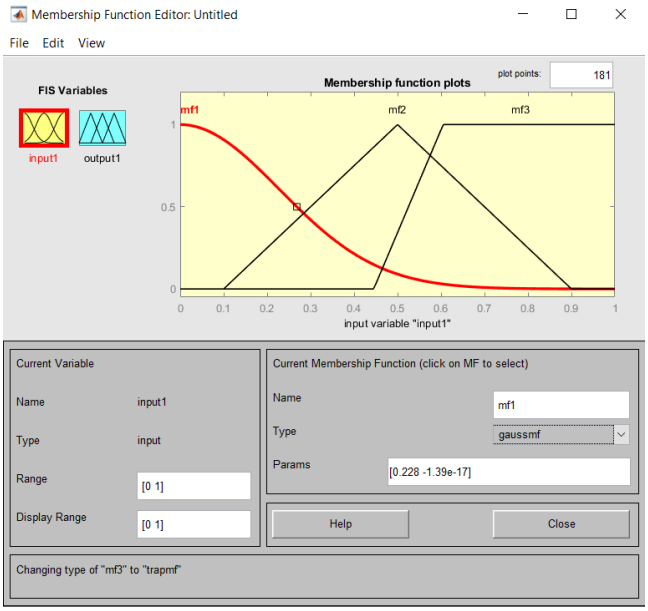



***Figure 5.4*** *Examples of membership functions provided in MATLAB for modelling FL.*

The type of curve selected has an impact on the end results but it is not the most important aspect. It is very important to select the right number of inputs and outputs as well as correctly specifying the overlapping nature between the curves in the universe of discourse [39] .

After fuzzification of the membership functions, a rule base is applied to them. This is the most important process of the FL fault detection. This is because the rules defined determine the accuracy of the solution presented by the fuzzy model. This involves modification of the linguistic variables using simple if-then rules. An example of a rule base statement applicable to the short circuits in this study is:
If $i_a$ is maximum and $i_b$ is normal and $i_c$ $is\ normal$ and $v_a$ is minimum and $v_b$ is normal and $v_c$ is normal, Then fault type is $lgsc$.
where each element has three defined states; minimum, normal and maximum.

The next step of designing the fuzzy model is defuzzification of the inference engine output. It entails assessing the correct value of the solution based on the 'membership-ness' of a variable. In general, the closer the value of a variable is to 1, the more contribution its membership function makes to the final output. This implies that variables with a score of 0.8 maybe considered to have a greater probability of being abnormal compared to a variable with a value of 0.32 on the 0 to 1 range of the universe of discourse. This value is normally determined by the inference engine and thus, it is very important to accurately define fuzzy rules. There are different methods of performing defuzzification, for instance, center of gravity and centroid techniques.

The final step involves testing the designed model by comparing the results the FL system gives of known outputs. For example, after performing a single line to ground fault, the system should give the accurate answer. The designed FL system could not successfully identify short circuit fault conditions using instantaneous values. This is because the set threshold values occurred once in every cycle of the sinusoidal input voltage and current. For every crossing of the threshold value in the sinusoid, FL reported a fault condition. This situation could be resolved using RMS values instead of the actual raw variables. However, this makes the fault detection scheme slower and the desired fault detection time of $100ms$ can not be achieved. Therefore, FL is suitable for certain applications, under limited conditions. For the requirements of this study, FL is not a suitable method.

## 5.3 Hybrid methods

High precision results in fault diagnosis can be ensured when several techniques are used to process information, perform problem solving and review the accuracy of results. Integrating different diagnosis techniques guarantees more conclusive results. Moreover, hybrid systems support the combination of methods with complementary strengths and weakness, creating a multifaceted system. This is especially popular for systems designed to perform both fault detection and classification. Two types of hybrid systems exist; a hybrid of two software methods or a hybrid of a software and a hardware method.

Examples of hybrid software methods are neuro-fuzzy and fuzzy-wavelet methods. The neuro-fuzzy method uses a combination of ANNs and FL to perform fault diagnosis while fuzzy-wavelet method is a combination of DWT and FL. These methods are very useful in big complex systems. Software- hardware hybrids are better suited for simpler power electronic systems which can be customized to the desired functionality. The selected

method discussed in subsection 5.4, is a hybrid of software and hardware methods for fault detection. The tripper circuit that gives the current spike to the CB forms the hardware section while the flow chart of Figure 5.5 shows the overview of the software detection scheme.

## 5.4 Implemented fault detection algorithm

It was crucial to come up with a customized alternative fault detection method after the unsuccessful implementation results from the FL detection algorithm. This customized method was designed to overcome the drawbacks discussed in the mainstream detection methods in subsections 5.2 and 5.3. The design process examines key factors like optimization of microprocessor resources, fast fault detection responses and reusability of existing UPS measurements as inputs. Subsection 5.4.1 reviews the implemented method in more detail.

The software algorithm is developed on the current platform used for the 93PS firmware. This method is customized to the response of the UPS systems during short circuits and has been developed through analysing simulated and laboratory test results of short circuit faults, overload conditions and transformer start up transients. The fault detection algorithm is based on the shape of the voltage and current waveforms during short circuits.

Figure 5.5 summarizes the working of the implemented detection algorithm and proposed classification algorithm. The classification algorithm is presented comprehensively in chapter 6. In Figure 5.5, the detection algorithm starts to run after the UPS system has initialized. The detection algorithm detects short circuits after the UPS system is online, with or without loads connected. This algorithm runs iteratively in a loop until a short circuit is detected in any of the UPS output phases. If a fault is detected, the tripper circuit is activated to isolate the relevant faulted phase(s). The proposed classification algorithm would then used to determine the type of short circuit fault that occurred.

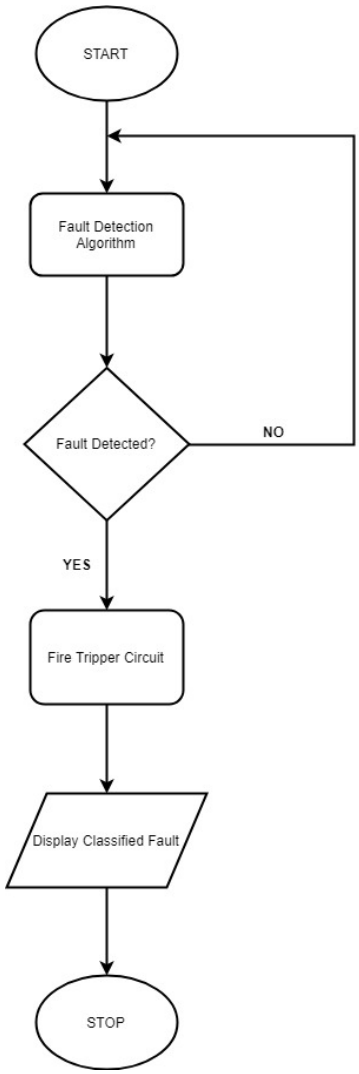



***Figure 5.5*** *Flowchart for general logic flow of the fault detection and classification algorithms.*

### 5.4.1 Detection Algorithm

The detection method utilizes instantaneous values to track the change in voltage and current values. Instantaneous values give the actual raw unfiltered measurements of the 93PS. This has a huge impact on the speed of response since it is possible to detect system abnormalities as they occur. The output current and voltage measurements utilized are readily available from the UPS system's meters.

The detection algorithm tracks the instantaneous output current and primarily bases its decisions on its state. From chapter 4 laboratory test waveforms, it is observed that the short circuit output current waveform is similar in all the four types of short circuits. It is a hardware limited square wave of $72A$, intended to provide protection to the inverter switches from overcurrent damage. The output current uniformity is a prime characteristic to leverage due to the ease of comparing the instantaneous current values to the preset inverter current limit. Several samples of the current value are taken and compared to the inverter current limit, if these values are equal within the acceptable tolerances, the output current is no longer sinusoidal and a fault is determined to have occurred.

Further analysis on voltage is then done to confirm that a short circuit has occurred as well as determine the type of short circuit.

In the flowchart of Figure 5.6, a more detailed description of the working of the algorithm is outlined. Several variables are used in the detection algorithm including input variables, number of samples and status flags. Input variables $i_a(t), i_b(t), i_c(t)$ represent the measured instantaneous output current values while $u_a(t), u_b(t), u_c(t)$ are the instantaneous output voltage values. A fault flag is a true or false value that is normally set to indicate the state of a monitored element. It is set to true when a condition is met and remains false otherwise.

The number of samples ($S$) of the output current to be taken are then set. The minimum number of sample values that can be taken is 2. This is done to eliminate occurrence of a false positive situation in case the current limit value is recorded during a normal instantaneous current when the output current is equal or greater than $72A$ or due to transients and noise. The sample size affects the speed of response of the algorithm since the time taken by the processor between two consecutive samples is approximately $0.88ms$. The desired speed of response to perform isolation of the detected fault is $100ms$. This includes the time it takes to detect the fault, send the signal to the tripper circuit and discharge the capacitor to trip the CB. It takes approximately a maximum of $12ms$ between the time the tripper circuit receives the activation signal to the time the CB isolates the faulted phase(s). If we assign a maximum of $30ms$ for detection, the maximum number of samples should not exceed 34. This is a huge sample size and therefore, this fault detection algorithm gives lot of flexibility for the user to set their desired sample size. A very small sample size may result into a false positive while a too high sample size slows down the speed of response. A sample size of between 5 and 13 is enough to successfully carry out the detection. Eight sample sizes are used in the designed system and the exact detection times for the single line to ground, line to line, double line to ground and three-phase faults are presented comprehensively in both subsection 7.3 and Appendix C.

When a short circuit happens, several samples of the current values are taken and compared to the known current limited value. If this value is the same, the instantaneous voltage values are then compared to the laboratory determined threshold value for each type of the short circuit. This is done for all the three-phases and depending on the type short circuit detected, the system sets the relevant flags. Flags $PHA\_short$, $PHB\_short$ and $PHC\_short$ are used to indicate a short circuit or ground fault in phases A, B and/or C respectively. The states of $PHA\_short$, $PHB\_short$ and $PHC\_short$ are then analysed and used to activate the tripper circuit for the faulted phase(s).

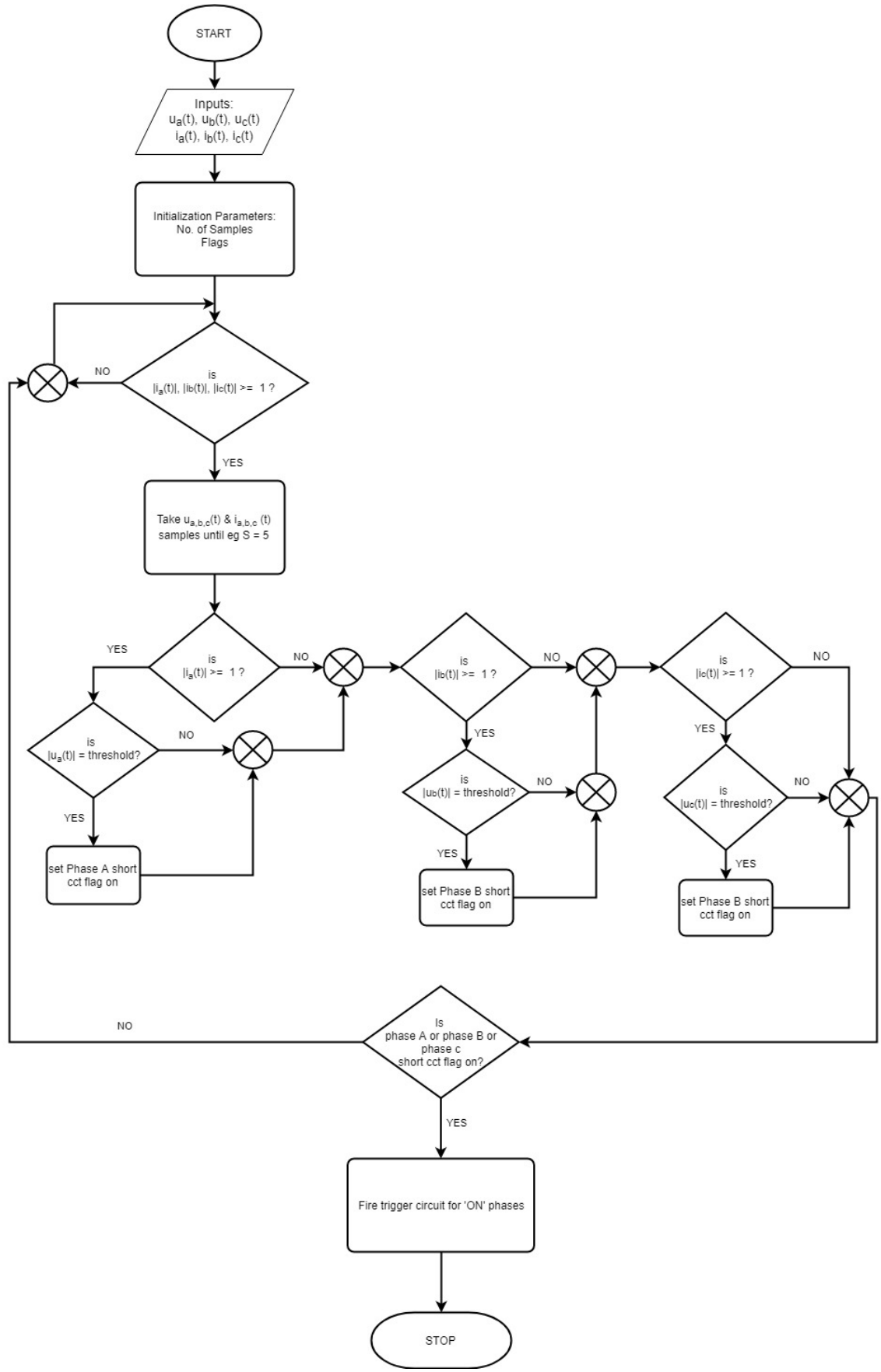



***Figure 5.6*** *Short circuit fault detection logic flowchart.*

# 6. FAULT CLASSIFICATION METHODS

Fault classification involves placing short circuit faults into their right categories using their distinctive qualities. This is especially beneficial in large and complex systems with numerous variables. Fault classification reduces the system downtime as well as increasing the efficiency of maintenance routines. Fault detection and classification methods are selected such that they are complementary to each other. This is because, the results from the fault detection algorithm are usually used to implement the classification algorithm. Therefore, algorithms based on one design platform have a logical progression from one state to the other, are simpler and more straightforward to implement, use resources more efficiently and are easily modified to accommodate new data [41] .

Fault classification techniques in power electronic systems are primarily software based and hence very flexible to adapt to needs while maintaining high system performance. The most widely used, well known classification techniques are wavelet transforms, ANNs and FL [41] . DWT, ANN and FL fault classification algorithms are generally implemented together with their respective fault detection methods. These methods have been examined in depth in chapter 5. A combination of these methods such as Neuro-fuzzy, wavelet and ANN, wavelet and fuzzy, wavelet and Neuro-fuzzy make up the hybrid methods. Although not proposed for implementation, a brief overview DWT, ANN,FL and hybrid techniques are presented in subsection 6.1, with regard to their application in fault classification. The proposed fault classification algorithm is then introduced and discussed in subsection 6.2. There exists other numerous techniques for fault classification, many still under development and research, designed for power systems [42] . Some of these methods have been applied to microgrids and synchronous motors and may also be adapted to some power electronic applications [43] .

## 6.1 Summary of fault classification techniques

DWT is a numerical signal processing technique suitable for analysing non-stationary signals. It possesses advanced fault feature extraction abilities with possibilities to give the accurate fault location as well as classify the fault. This is done by decomposing the signal to be analysed into wavelets using techniques such as, Multiresolution analysis (MRA). MRA decomposes a signal into an approximated version by low pass filtering and a detailed version using a high pass filter. Scaling factors and their accompanying wavelet coefficients are then calculated. The coefficients calculations can be made based on fault currents frequency content or wavelet energy levels as examples. Analysis is then performed on these coefficients using methods like standard deviation, mean and variance analysis. The coefficient analysis yields different numerical results for each type of short circuits which can be used to distinguish and classify these faults [41] . Although a very accurate method for fault classification, this technique is not proposed for implementation in fault classification due to the complex computations associated with the design process.

Fault classification by ANN is performed by training the algorithms to identify patterns in the variable chosen its input. The system is fed with pre-fault data that represents the normal operation and post fault data of the faulted system. For example, instantaneous voltage and current values can be used for short circuit fault classification. Different techniques exist on how to process this data for use in classification. One common approach involves calculating per unit values by dividing the faulted system values with values from the system during normal operation. The ANN then categorizes the fault types, based on the per unit values, using the process illustrated in Figure 5.1. Due to their demand of processor resources, ANNs are implemented using Field Programmable Gate Arrays (FPGA) which have enhanced processing capabilities compared to Digital Signal Processors (DSP). A DSP is a microprocessor specialized to perform a certain function while FPGA is a highly configurable hardware designed to process a higher quantity of instructions per second compared to the DSP [44] . The 93PS UPS system uses DSPs and therefore implementation of ANNs is not feasible due to its resource intensive nature.

Subsection 5.2.2 B depicts FL fault classification by applying the rule base to membership functions. FL fault classification is simple and easily understood because the fuzzy IF-THEN rules use linguistic terms that are similar to spoken language. The fault conditions in this study can be completely represented using 10 IF-THEN rule statements as can be gathered from the fault states in Table 4 and Table 5. Due to its simplistic implementation nature, FL has gained approval for application on many platforms [41] . However, if the systems are very complex with many inputs, coming up with a rule base for all conditions could be quite tedious. Implementation of FL classification goes in tandem with the FL detection algorithm since its inputs are the outputs of the FL algorithm. Thus, FL classification is not recommended as a suitable method for this study.

Hybrid methods are meant to overcome the limitations of one technique through integration with a complementary method. They are combined such that one hybrid techniques performs fault detection and the other is used for classification. This way, desirable qualities from the hybrid techniques are leveraged to reduce complexity of the design, ensure efficiency of resources and maximize algorithm adaptability and reliability [41] . Based on the number of algorithm inputs and computations, FL and hybrids involving it, are considered the simplest systems for implementation in suitable applications [41] .

## 6.2 Proposed classification algorithm

The flowchart of Figure 6.1 illustrates the proposed comprehensive logic used to classify the type of fault that has been detected. This algorithm is intended to be developed on the same platform as the implemented detection algorithm. Since the input to the classification algorithm are flags set by the detection algorithm, classification is done after fault detection to aid in debugging a faulty UPS system. The classification algorithm operates as a two part process; first the flags for the faulted phases are set and secondly, they are analysed and the fault type determined depending on the state of the flags. This two-part process is expounded in step i and step ii below.

**i.** Setting system flags

$PHA\_short$, $PHB\_short$ and $PHC\_short$ are the input flags to the classification algorithm from the detection algorithm. They indicate the phase(s) in which the short circuit or ground fault was detected. In the classification algorithm, seven flags have been selected to describe the state of the UPS system during short circuits or ground faults. They include $3PH\_g$ which is set high when there is a three-phase to ground fault, $PhA\_L, PhB\_L, PhC\_L$ are the individual line short circuit faults for phases A, B and C respectively and $PhA\_g, PhB\_g, PhC\_g$ represent line to ground fault in phases A, B and C respectively. $PHA\_short$, $PHB\_short$ and $PHC\_short$ determine the states of these seven flags.

Table 3 gives the logical process followed in activating the classification algorithm flags. The classification process begins with analysing if $PHA\_short$, $PHB\_short$ and $PHC\_short$ flags are all set high. If all the flags are high, $3PH\_g$ is set high. If not all the flags were determined to be high, each phase flag is checked individually and its voltage level analysed to establish whether a line to line short circuit or ground fault has occurred. For example, if $PHA\_short$ is set high, peak value of phase A voltage is analysed. When the peak value is within the lower threshold, a ground fault has occurred and $PhA\_g$ is set high, if the peak voltage lies within the upper threshold, a line to line fault has occurred and $PhA\_L$ is set high. Similarly, $PHB\_short$, $PHC\_short$ and their respective voltages are analysed after which the proper flags $PhB\_g, PhB\_L, PhC\_g$ or $PhC\_L$ are set. The seven short circuits fault flags are activated individually and then analysed in step ii.

**ii.** Analysing the state of set flags

This is the second step that concludes what type of fault has occurred through analysing the state flags. It is a logical process that is summarised by Table 4 and Table 5. The process starts with checking whether $3PH\_g$ flag has been set high, if this condition is true a three-phase to ground fault is reported. If false, $PhA\_L$ $PhB\_L$ and $PhC\_L$ are examined to determine whether any of their states are high. The fault type is then reported according to Table 5. When only $PhA\_L$ and $PhB\_L$ are high, a double line fault involving phases A and B is reported. If only flags $PhA\_L$ and $PhC\_L$ are set high, the double line fault has occurred in phases A and C and a double line fault in phases B and C is indicated when only flags $PhB\_L$ and $PhC\_L$ are high.

If neither of the line fault flags are high, $PhA\_g, PhB\_g$ and $PhC\_g$ are checked and their states compared as represented in Table 4. A state where only $PhA\_g$ is high indicates phase A to ground fault. Similarly, Phase B to ground and phase C to ground faults are denoted by the high state of only $PhB\_g$ and only $PhC\_g$ respectively. Furthermore, when only $PhA\_g$ and $PhB\_g$ are high, it indicates occurrence of a double line to ground fault involving phases A and B. When only flags $PhA\_g$ and $PhC\_g$ are set to high, it represents a double line to ground fault in phases A and C. A double line to ground fault in phases B and C is defined by having only $PhB\_g$ and $PhC\_g$ set to high.

***Table 3.*** *Short circuit to ground faults truth table.*

| State of flag | | | |
|---|---|---|---|
| $PHA\_short$ | $PHB\_short$ | $PHC\_short$ | **Set flag** |
| 0 | 0 | 1 | $PhC\_g$ / $PhC\_L$ |
| 0 | 1 | 0 | $PhB\_g$ / $PhB\_L$ |
| 1 | 0 | 0 | $PhA\_g$ / $PhA\_L$ |
| 1 | 1 | 1 | $3PH\_g$ |

***Table 4.*** *Short circuit to ground faults truth table.*

| State of flag | | | |
|---|---|---|---|
| $PhA\_g$ | $PhB\_g$ | $PhC\_g$ | **Fault type** |
| 0 | 0 | 1 | *Phase C to ground* |
| 0 | 1 | 0 | *Phase B to ground* |
| 0 | 1 | 1 | *Phase B to phase C to ground* |
| 1 | 0 | 0 | *Phase A to ground* |
| 1 | 0 | 1 | *Phase A to phase C to ground* |
| 1 | 1 | 0 | *Phase A to phase B to ground* |

***Table 5.*** *Double line faults truth table.*

| State of flag | | | |
|---|---|---|---|
| $PhA\_L$ | $PhB\_L$ | $PhC\_L$ | **Fault type** |
| 1 | 1 | 0 | *Phase A to Phase B fault* |
| 1 | 0 | 1 | *Phase A to Phase C fault* |
| 0 | 1 | 1 | *Phase B to Phase C fault* |

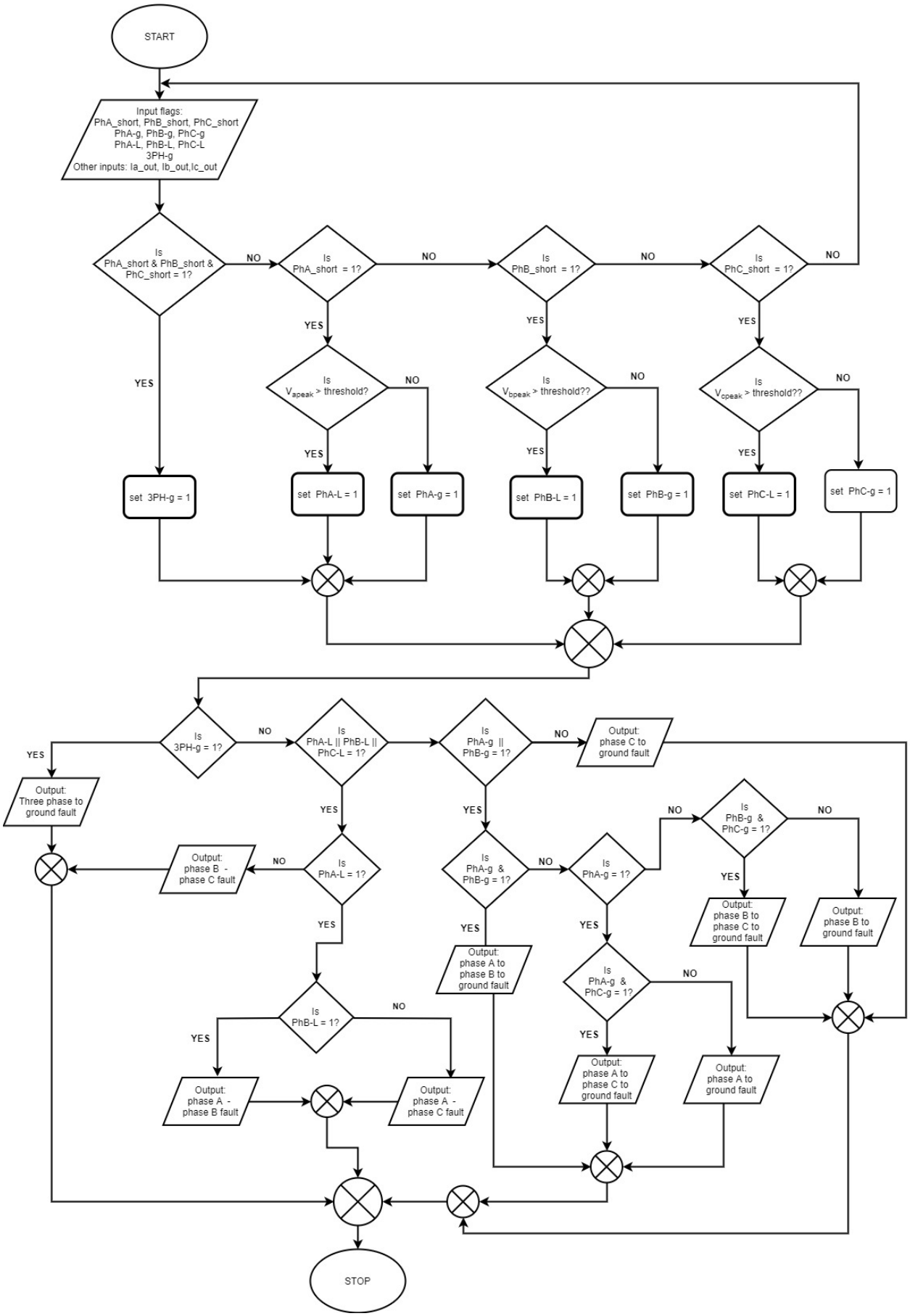



***Figure 6.1*** *Short circuit fault classification logic flowchart.*

# 7. SIMULATION AND LABORATORY TESTS AND RESULTS

The MATLAB simulations, laboratory short circuit test results on a real 93PS unit and short circuit detection results on an actual 93PS unit are presented in this chapter. In subsection 7.1, a simulation model developed using Mathwork's Simulink is introduced, its functioning explained and relevant figures included in Appendix A. The Simulink model was developed based on Eaton's 93PS 20kVA UPS system. This was done as part of the preliminary studies in conjunction with literature review on different fault detection techniques. The purpose of developing the model was to study voltage and current behaviour in simulated short circuit fault waveforms. The general current and voltage response during faults was then compared and contrasted to the unique features possessed by the input variables in the analysed fault detection methods. If many similarities existed between the short circuit simulations and a detection method, it signified an increased likelihood of successful implementation and vice versa. Subsection 7.2 describes similar tests to the simulations conducted on an actual 93PS 20kVA unit in the laboratory. These short circuit tests were done to compare the simulations with results from a real system. Comparisons between the results from the simulations and laboratory have been presented and discussed in chapter 4. The laboratory test setup is demonstrated and raw data from the scope setup of the 93PS unit is included in Appendix B. Results from the implemented detection algorithm are discussed in subsection 7.3 and acquired waveforms presented in Appendix C.

## 7.1 Simulation Model

This is a simplified three-phase model consisting of an inverter, its control circuit and different load configurations used to simulate line to ground, double line to ground, line-to-line and three-phase to ground faults. The model is composed of two major subsystems and a scope as shown in Appendix A, Figure 1 with a simulation time of $1$ second. The first subsystem is the inverter control system and the second one comprises the simplified inverter with different load configurations.

Figure 2 in Appendix A illustrates the circuitry of the simplified inverter control circuit. The input values of this subsystem consist of a three-phase sinusoidal signal that serves as the reference and the three-phase feedback instantaneous voltage from inverter output terminals (subsystem two). The sinusoidal reference represents ideal AC supply voltage of peak value $325V$ and frequency $50Hz$ per phase. The difference between the reference signal and the feedback output voltage is calculated by performing a subtraction and the result fed to a transfer function. The dynamic modelling of the inverter has been simplified by using the transfer function that is represented as a numerator and denominator ratio. The transfer function converts the computed voltage difference to current values that are fed to the constant current source that simulates an inverter in subsystem two. The transfer function has been designed for a load value that gives a current value

of $40.85A$ during normal operation and an overcurrent of $21.4kA$ during a short circuit. The current values can be changed by setting the desired transfer function. The transfer function output is then fed to the saturation blocks which subject it the upper and lower inverter current limit values. The hardware defined inverter current limit value in this case is $72A$. Therefore, as can be seen from the Simulink figures of chapter 4, inverter current is $40.85A$ during normal operation and $72A$ when short circuits and ground faults occur. The next step involves determining the switching pattern of the inverter. If it is desired to keep the inverter on during the whole simulation period, a product of the output of the saturation box and an inverter 'ON' signal (logical high) from $inv\_on$ node forms the output of subsystem one. To start the inverter in off state, logical low signal is multiplied with the saturation block output while a step function with the defined step time is used to specify the switching time of the inverter on and off states.

Subsystem two is divided into 3 blocks each consisting of a constant current source and different load configurations. There are three constant current sources, for a three-phase system, fed by the current waveform output signals of subsystem one. The constant current sources represent an inverter. In Block 1, shown in Figure 3 Appendix A, two faults are simulated for the given load configuration. A single phase to ground fault is simulated for phase A and occurs between $0.2 - 0.4\ s$ while a double line fault between phases A and B is simulated between $0.5 - 0.8\ s$. Figure 4 in Appendix A gives the configuration of block 2. A three-phase to ground fault is simulated between $0.3 - 0.6s$ while overloading in phase B is simulated between $0.8 - 1s$. Block 3 is shown in Figure 5 of Appendix A, where a double line to ground fault has been simulated in phases A and B between $0.3 - 1s$. The rest of the time when faults are not simulated, the output is that of a normal 'healthy' UPS system. In all the simulated faults, the period of transition from normal functioning to the fault state is captured in Simulink figures presented in chapter 4.

## 7.2 Laboratory setup

Figure 7.1 illustrates the laboratory setup for the 93PS unit used in this study. The main elements are the UPS system, a tripper circuit, a short circuit box and an oscilloscope. The UPS system, oscilloscope and the short circuit box all have separate sources. They are all fed from three-phase supplies of $400V$ line to line and frequency $50Hz$ in phases A, B and C. The load connected to the UPS system is resistive in nature and can be added step wisely. The tripper circuit is treated as a black box.

The 93PS unit is a $20kW$ double conversion UPS system with the main components and operation as given in subsection 2.1.1. The main focus of this study is the UPS downstream made up of the inverter and the critical load. The inverter is an NPC, PWM controlled converter with IGBTs operating at 18kHz switching frequency.

A Yokagawa DL850 model oscilloscope has been used to view voltage, current and detection signal waveforms. Waveforms presented in chapter 4 have been filtered by the

oscilloscope at 300Hz to filter out noise for better clarity of explanation. Similar raw unfiltered laboratory test results are presented in Appendix B. A table has been included that gives a brief description of the waveforms.


***Figure 7.1*** *Laboratory setup for the 93PS unit.*

Figure 7.2 shows the wiring of the short circuit box. Its input terminals are connected to the output of the UPS at the same connection point as the critical load. The output side terminals are used to configure the short circuits and ground faults. For example in the figure, T1 and T2 are connected via a short cable used to test line to line fault. Two short cables were used to configure the various faults to the output side terminals. They have a resistance value of $0.4\Omega$.

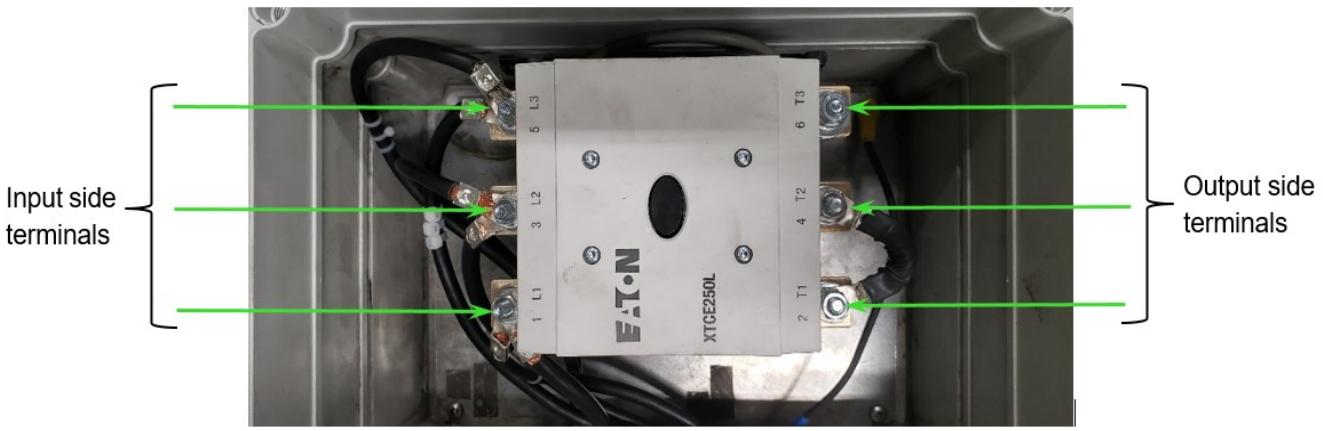



***Figure 7.2*** *Short circuit box wiring.*

To initiate the tested short circuit and ground faults, the desired fault is wired at the short circuit box output side terminals. The neutral wire from the NPC inverter is used as the ground terminal where the short circuit current flows during a fault. Next, the 93PS unit is powered and operated in normal mode with the scope set to trigger mode. The short circuit box is then powered from the grid causing the contactor to switch on and the input side terminal of the short circuit box are connected to the output side terminals thereby

causing the short circuits. The current and voltage waveforms of this process are presented in Figure 1, Figure 2, Figure 3 and Figure 4 included in Appendix B.

The overloading tests were performed by adding the resistive load to the UPS output in steps. A $33kW$ load was connected for the overload test illustrated in Figure 4.9 (b). The effect of adding a load step to the current can be noted in all phases where there is a sharp rise in the current when load is increased and a corresponding sharp deep and quick recovery in the voltages of phases A and B is observed. The laboratory testing exercises were carried out adhering to safety standards and using correct protective equipment.

## 7.3 Results of the detection algorithm

The implemented detection algorithm can be presented as the pseudocode of Figure 7.3. The developed algorithm uses pre-existing measurements of the 93PS and is optimized to run on the existing software platform. The detection times of this algorithm are presented in this section.

```
function ThreePhaseShortCircuitDetection(instantaneous current, instantaneous voltage, normalization factor)
{

  calculate the absolute normalized value for instantaneous voltages per phase
  calculate the absolute normalized value for instantaneous currents per phase

  check the normalized current for inverter current limit
  if limit is reached
  {
    check 8 samples of current to confirm current limit reached
    if current limit is reached
    {
      check 8 samples of voltage to confirm it is within the threshold
      if within threshold
      {
        set relevant flags
       }
     }
  }

  check the fault flags and activate the correct detection signal to DSP
  reset signal when fault flags are cleared
}


{
  In main fucntion

  call by reference function ThreePhaseShortCircuitDetection
  pass actual parameters from UPS meters
```

***Figure 7.3*** *Detection algorithm pseudocode.*

Experimental tests for the short circuits, ground faults and overloading described in subsection 7.2 are repeated when the 93PS unit software is updated with the detection algorithm. Three detection signals denoted as $short\_A, short\_B$ and $short\_C$ are used to indicate when a short circuit has occurred in phases A, B and C respectively. These signals are used to aid in visual detection and estimation of the total time taken to detect the faults. These signals are initialized to a high state (logical 1) and transition to a low

state (logical 0) when a short or ground fault is detected. The signals are acquired from the selected legs on a microprocessor chip and then displayed on the oscilloscope.

The detection tests were carried out with a load of $12kW$ and with no load connected. This is because the detection algorithm is expected to detect short circuits and ground faults with and without a load connection. If a short or ground fault occurs when the load is not connected, fault isolation and clearing should be activated to prevent connection of the sensitive load to the faulted phase. The voltage and current waveforms are identical in the loaded and unloaded cases except that output current does not exist before the point of fault in unloaded cases. Appendix C contains waveforms from the loaded scenario because it can exhaustively represent both cases.

From figures in Appendix C, it is clear that the detection algorithm works successfully and it is possible to determine in what phase the fault has occurred through the activation of the detection signals. Since it is possible to determine in which phase the overcurrent fault has occurred, it is possible to perform localized fault isolation. The voltage and current waveforms together with the detection signals are presented in detail from Figure 1 to Figure 16 in Appendix C.

The total time taken by the detection algorithm is a very important parameter in this study. This is due to the imposed requirement of a desired time of response of less than 100ms. The total time of detection is affected by factors such as exact instance of occurrence of the fault (beginning, middle or end of the positive or negative cycle), the $120^{\circ}$ phase shift between three-phase signals and the transients and noise that occur during the fault, causing the current and voltage to fluctuate rapidly. To ascertain the detection times, the detection signals of a loaded and unloaded 93PS unit will be briefly presented in the order of the most frequently occurring fault. The presentation of a loaded and unloaded case is not for comparison of the detection times. The purpose to give two different example cases and a projection of the predicted times of responses. This is because, it is not possible under the current setup, to replicate the exact instant of fault occurrence in the two cases and therefore, the detection times cannot be directly compared.

A single phase to ground fault in phase A was initiated and the waveforms recorded as can be seen in Figure 1, Appendix C. Figure 7.4 (a) shows a detection time of $2.140ms$ for this fault when a $12kW$ loads is connected and a detection time of $10.100ms$ in Figure 7.4 (b) when no load is connected to the UPS system. The time variation may be due to the difference in time of occurrence with regard to the positive or negative cycle of the two faults. The detection time is determined by observing how long the detection signal is triggered after a short or ground fault is initialized. It can also be observed in Figure 2 of Appendix C that only signal $short\_A$ has been activated while $short\_B$ and $short\_C$ remain in their earlier states as seen in Figure 3 of Appendix C.

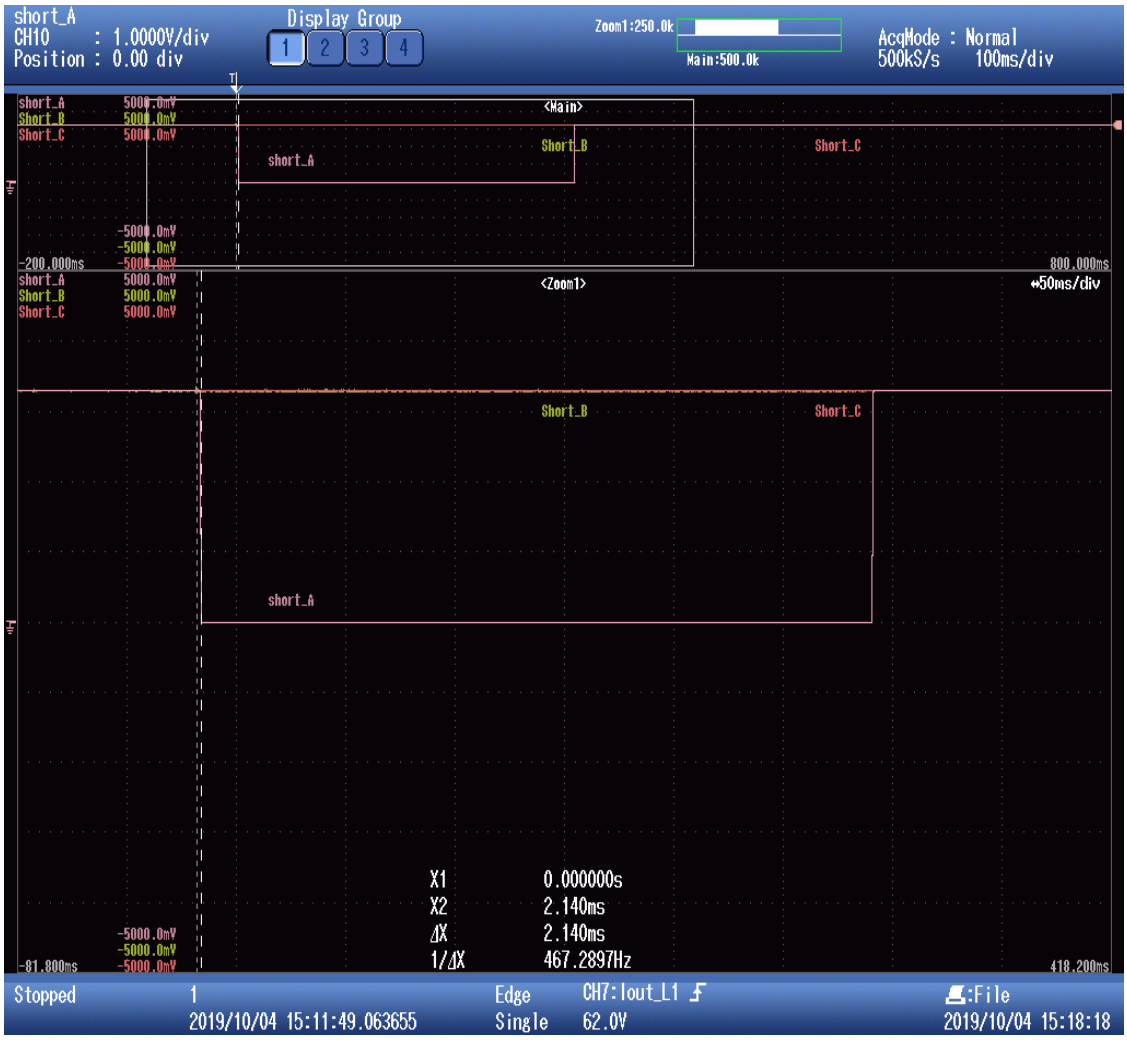



***Figure 7.4 (a)*** *single phase to ground fault detection time with* $12kW$ *load.*

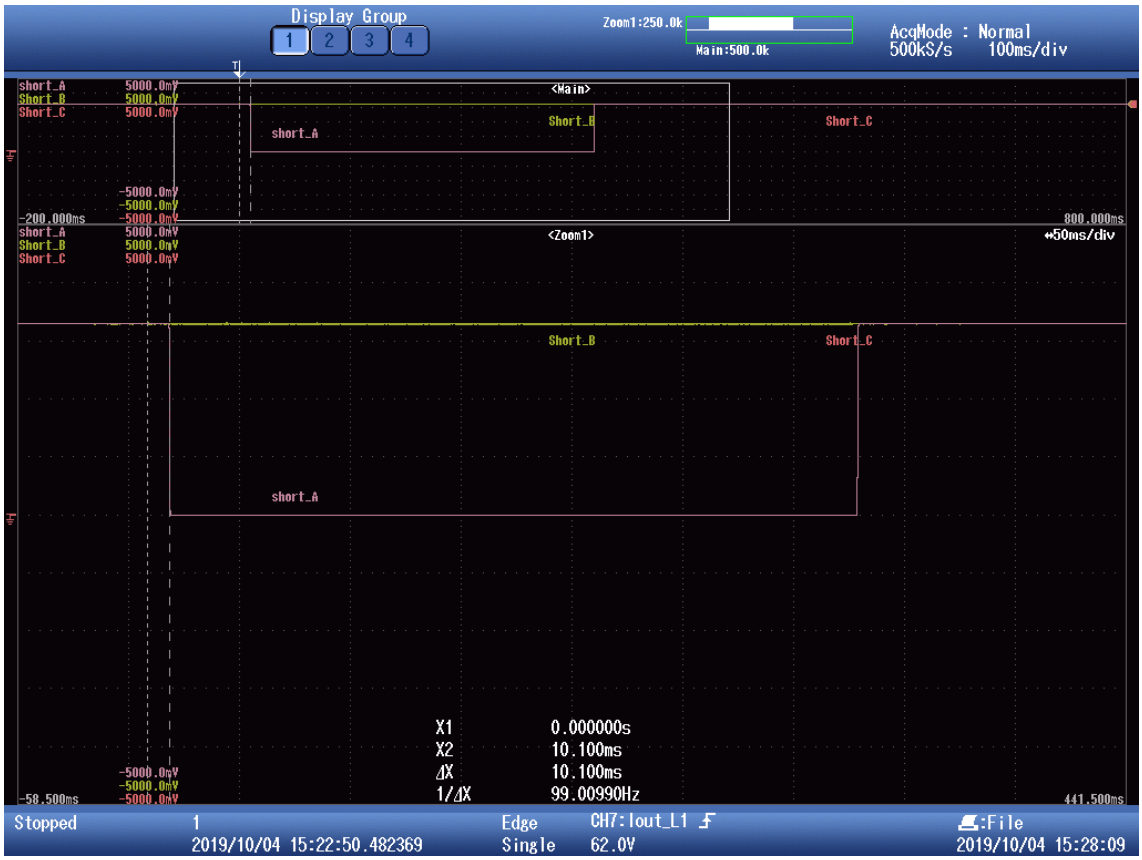



***Figure 7.4 (b)*** *single phase to ground fault detection time with no load.*

A line to line fault was then performed for phases A and B as illustrated in Figure 4 of Appendix C. The detection times for the loaded and unloaded cases are presented in Figure 7.5 (a) and (b) respectively. Figure 7.5 (a) gives the detection time of a line to line fault when the $12kW$ load is connected as $5.326ms$ in phase A and $15.200ms$ in phase B. In Figure 7.5 (b), the detection time for the line to line fault in phase A is $13.150ms$ while phase B has a detection time of $12.926ms$ without load.

It takes significantly longer for line to line fault detection compared to ground faults. This is due to the sharp sudden rises in the voltage thus making the threshold value exist for a shorter duration of time. This time can be considerably reduced by raising the voltage threshold value and evaluating the impact of this change on the detection times of the other faults as well. The sudden voltage spikes are also responsible for the detection signals changing state multiple times. This is however not an issue since successive fault detections after the first one are disregarded because the capacitors in the tripper circuit can only be discharged once per phase when a fault is detected until the capacitors recharge.

It is important to mention that for faults that involve more than one phase, the total detection time is equal to the longest time taken for fault detection. For example in the loaded case presented in Figure 7.5 (a), the detection time would be $15.200ms$ while the detection time for the case presented in Figure 7.5 (b) would be $13.150ms$. This is because, the tripper circuit is designed to be fired only once in the faulted phase(s) to clear the fault.

Only the $short\_A$ and $short\_B$ transition to active states while $short\_C$ remains in its the initial state. This is illustrated in Figure 5, Figure 6 and Figure 7 contained Appendix C, respectively.


***Figure 7.5 (a)*** *Line to line fault detection time with* $12kW$ *load.*


***Figure 7.5 (b)*** *Line to line fault detection time with no load.*

Figure 8 in Appendix C shows a double line to ground fault in phases A and B. The detection times when the UPS system has a $12kW$ load connected has been presented in Figure 7.6 (a). Phase A has a detection time of $2.826ms$ while $short\_B$ is activated in $2.526ms$. When 93PS unit is unloaded, $short\_A$ is activated in $2.826ms$ and $short\_B$ in $4.900\text{ms}$ as shown in Figure 7.6 (b). Therefore, the detection time for the loaded case is $2.826ms$ while the unloaded case has a detection time of $4.900ms$.

Figure 9 and Figure 10 in Appendix C show that the faulted phases detection signals $short\_A$ and $short\_B$ are activated while the detection signal in the healthy phase C remains undisturbed as depicted in Figure 11 of Appendix C.

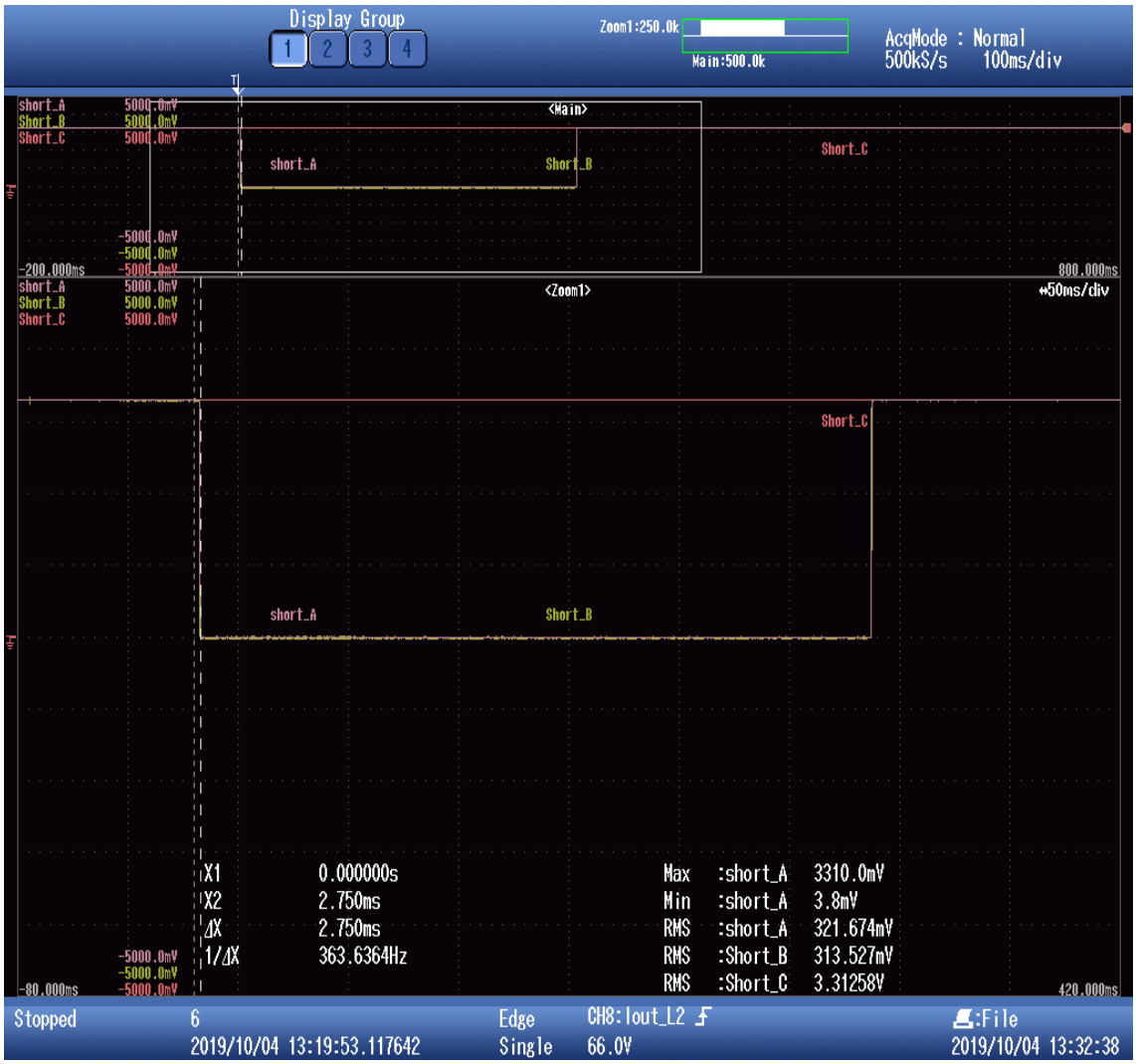



***Figure 7.6 (a)*** *Double line to ground fault detection time with* $12kW$ *load.*


***Figure 7.6 (b)*** *Double line to ground fault detection time with no load.*

Results of a three-phase to ground laboratory test on the 93PS unit are presented in Figure 12, Figure 13, Figure 14 and Figure 15 in Appendix C. It is observed that the detectors in all the three faulted phases have been activated. The detection times for the $12kW$ loaded case are presented in Figure 7.7 (a) while the unloaded detection times are presented in Figure 7.7 (b). In the case of the loaded system, the detection times are $5.150ms$, $2.926ms$ and $2.226ms$ for phase A, B and C respectively. The detection times for the unloaded cases were recorded as $3.726ms$, $2.626ms$ and $4.626ms$ for phase A, B and C respectively. The overall detection time for the loaded case would be $5.150ms$ while that of the unloaded case would be $4.626ms$.

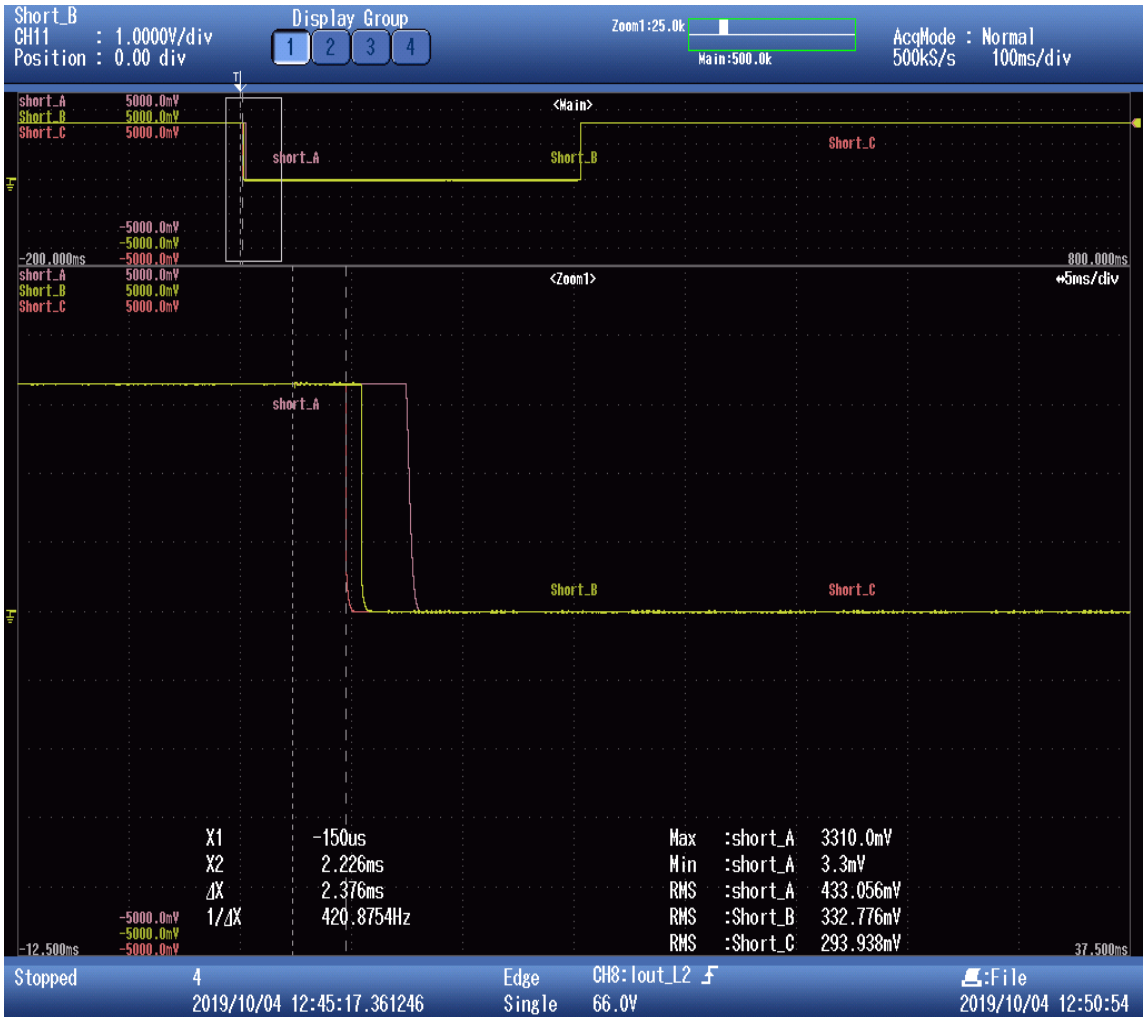



***Figure 7.7 (a)*** *Three-phase to ground fault detection time with* $12kW$ *load.*

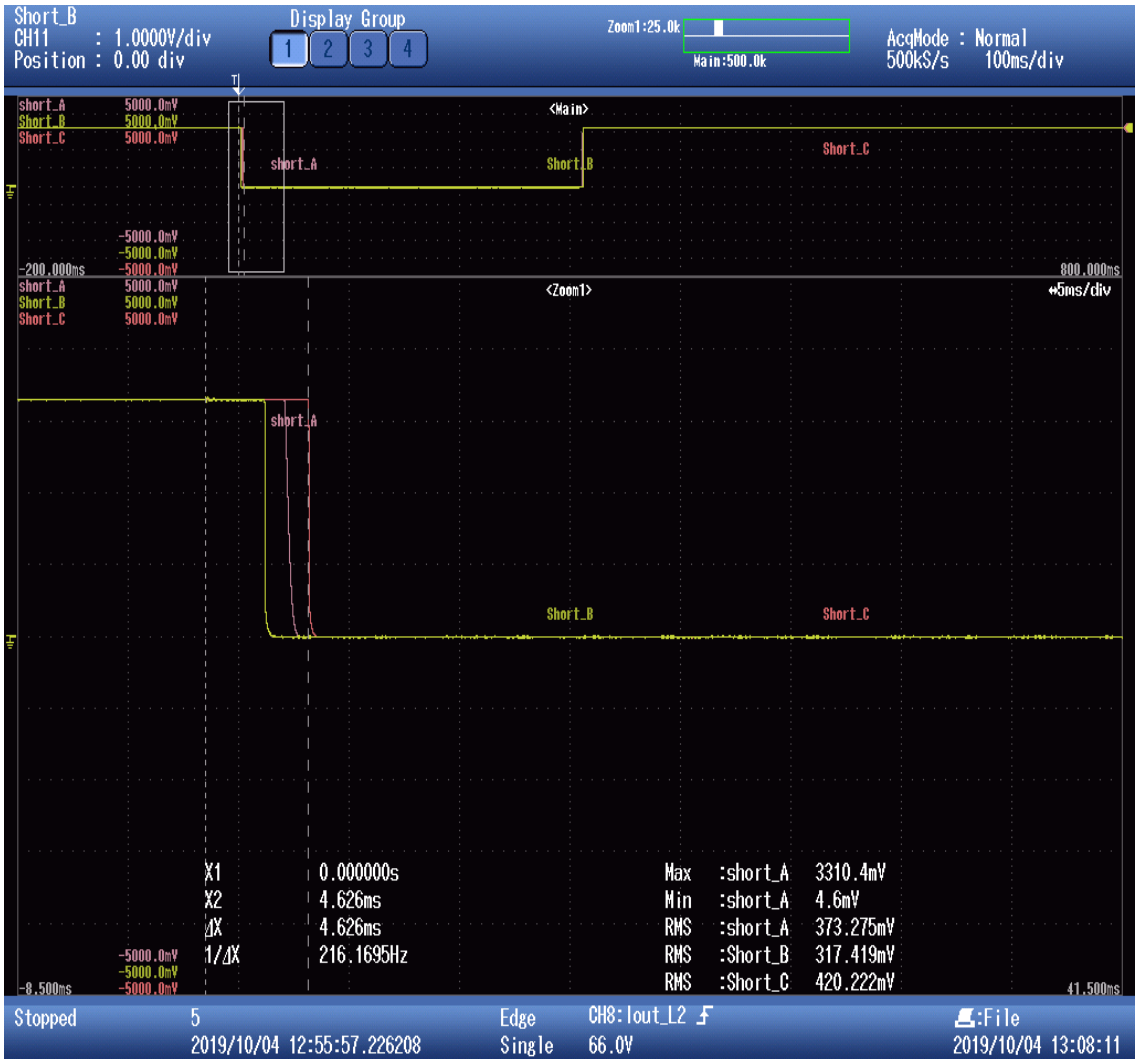



***Figure 7.7 (b)*** *Three-phase to ground fault detection time with no load.*

In Appendix C, Figure 16 shows the behaviour of the detection algorithm when the UPS system has an overload of $33kW$. It is observed that the detectors remain in their states and the algorithm can clearly discriminate overloads from short circuit faults.

Table 6 presents a summary of the detection times from the laboratory testing presented in this subsection. It can be observed that all the times recorded are well below the $100ms$ requirement. This shows that the detection algorithm implemented has good speed of response.

***Table 6.*** *Detection times summary*

| Fault type | Detection Time (ms) $12kW$ load | | | Detection Time (ms) Unloaded | | |
|---|---|---|---|---|---|---|
| | $short\_A$ | $short\_B$ | $short\_C$ | $short\_A$ | $short\_B$ | $short\_C$ |
| Single phase to ground | 2.140 | - | - | 10.100 | - | - |
| Line-to-line | 5.326 | 15.200 | - | 13.150 | 12.926 | - |
| Double line to ground | 2.826 | 2.526 | - | 2.826 | 4.900 | - |
| Three-phase to ground | 5.150 | 2.926 | 2.226 | 3.726 | 2.626 | 4.626 |

The main disadvantage of this fault detection algorithm is its reliability on threshold values that have been set through laboratory testing. This drawback has a greater impact when the instantaneous voltage and current values have a lot of distortions or transients. The impact of distortions can however be reduced through a small raise in the threshold values.

The advantages of the implemented scheme however far outweigh the disadvantages. To start with, the speed of response is well within the desired time for all the tested cases as can be seen from Table 6. Secondly, the detection algorithm has been developed using variables measurements already available from the UPS system which is both efficient and convenient. Additionally, the implemented detection algorithm is very simple and thus a good technique in embedded systems such as UPS systems where microprocessor resources are scarce. Moreover, there is a lot of flexibility that can be offered by the detection method as it allows customization to a customer's needs. This can be done by changing factors such as sample size and threshold values in order to set the time taken to detect a fault.

# 8. CONCLUSIONS

UPS systems are used to provide continuous and conditioned power to sensitive loads. To ensure critical loads are supplied with steady and reliable power, it is essential to perform continuous UPS system monitoring. Fault detection is a system monitoring technique that ensures that faulted phase(s) are isolated immediately to prevent cascaded loss of power in healthy phases supporting vital loads. With many existing detection methods, it can be challenging to find a suitable detection method, fitting a specific application. However, with careful analysis of system behaviour before, during and after a fault occurs, an efficient and effective method can be selected.

In this study, a detection algorithm that can successfully identify short circuits and ground faults was developed, implemented and the results tested in a real UPS system. The implemented algorithm can effectively differentiate short circuits and ground faults from other overcurrent faults such as overloading. In the designed algorithm, it was required to detect a fault in less than $100ms$. This is because the internal UPS OCP is activated after $300ms$. This causes the UPS system to trip, leading to loss of power to all loads. The time of response of the detection algorithm is well below $100ms$. Based on these results, this study was a success and the main objectives were achieved satisfactorily.

A fault classification algorithm was also proposed to aid in UPS debugging processes. This study is part of an ongoing project and the detection algorithm will be further refined as well as developed to activate the tripper circuit for fault isolation. The proposed fault classification algorithm will also be implemented.

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# APPENDICES

## Appendix A : Simulink model for load overcurrent tests

The Simulink model developed for the load overcurrent conditions is illustrated in this appendix. The table below contains descriptions of the models.

| Figure | Description |
|---|---|
| 1 | Simulink model inputs, subsystems and outputs |
| 2 | Simplified inverter control circuit |
| 3 | Inverter with load side single phase to ground and double line faults |
| 4 | Inverter with load side three-phase to ground fault and overloading |
| 5 | Inverter with load side double line to ground fault |

***Figure 1***

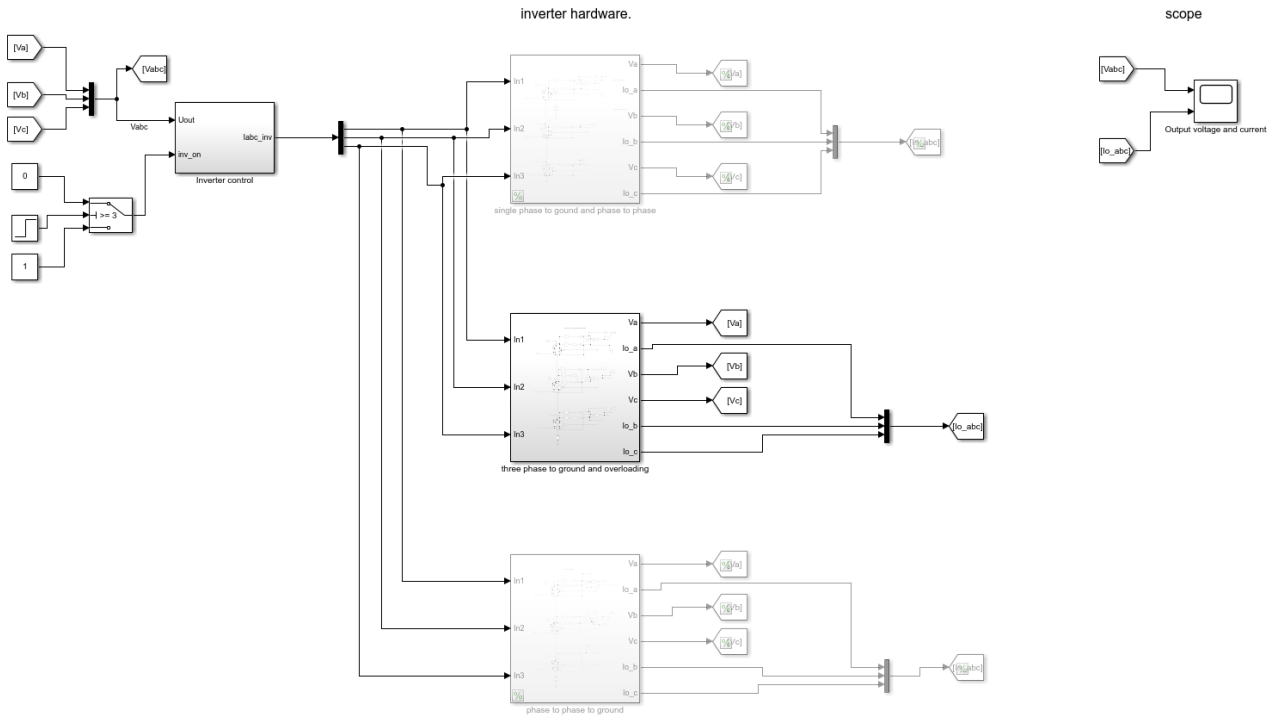


***Figure 2***

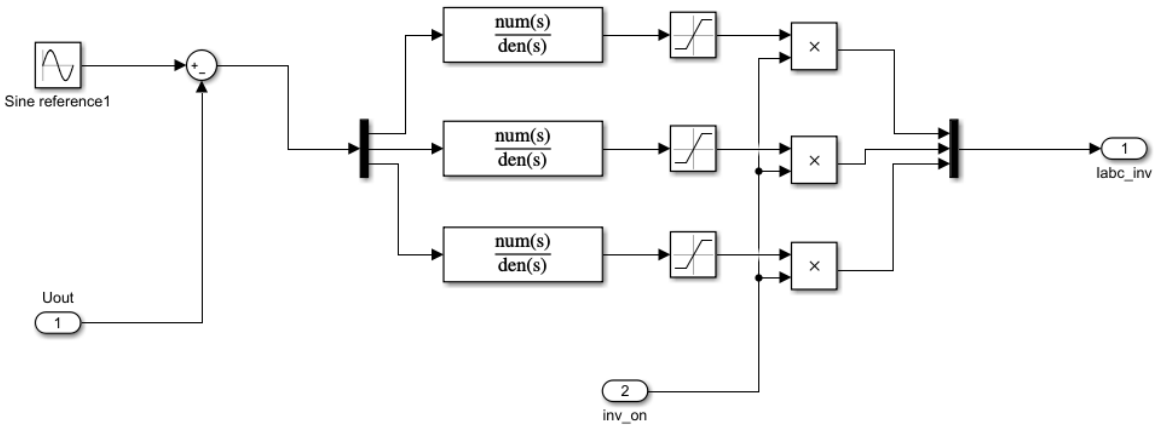



***Figure 3***

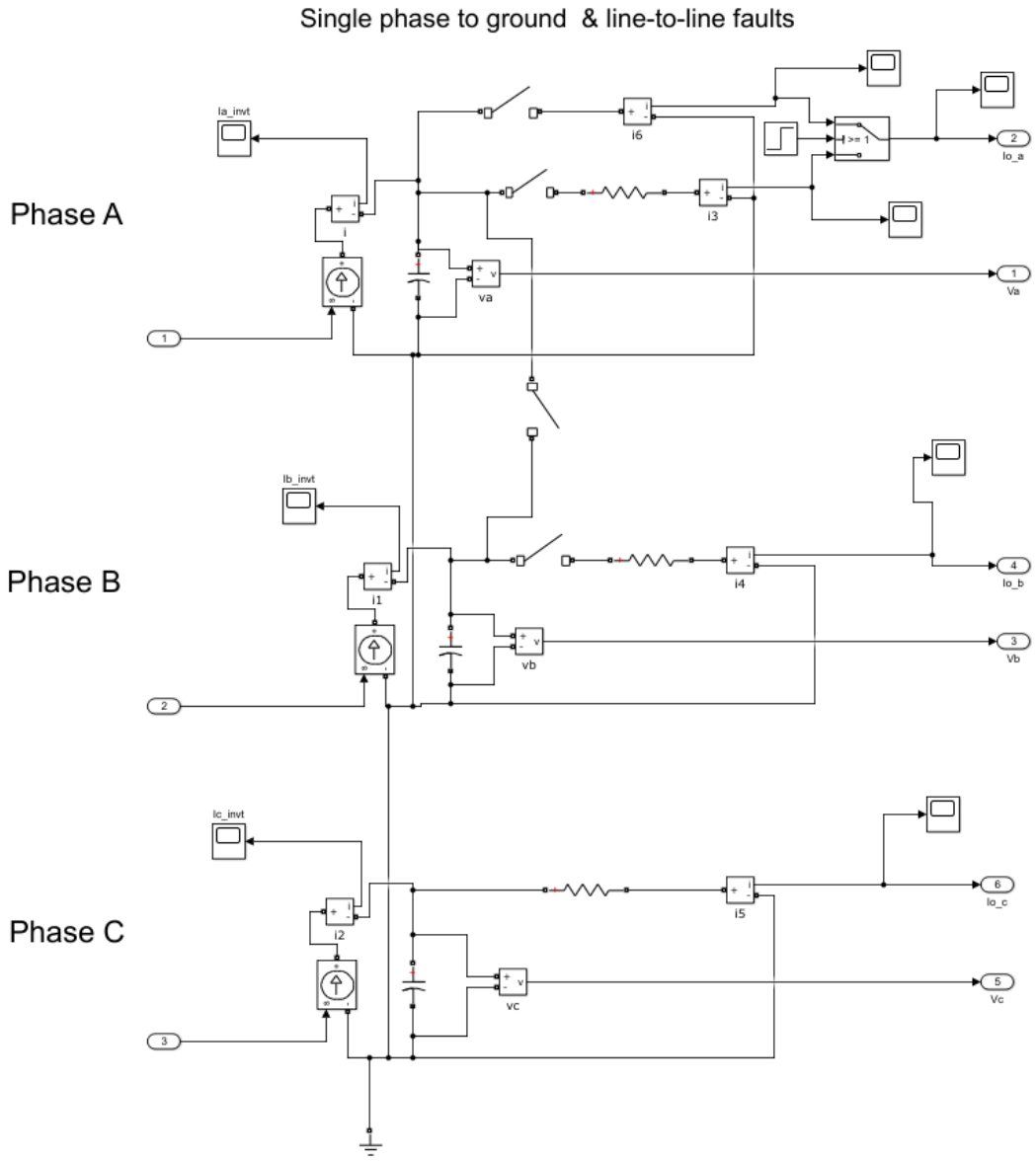


***Figure 4***

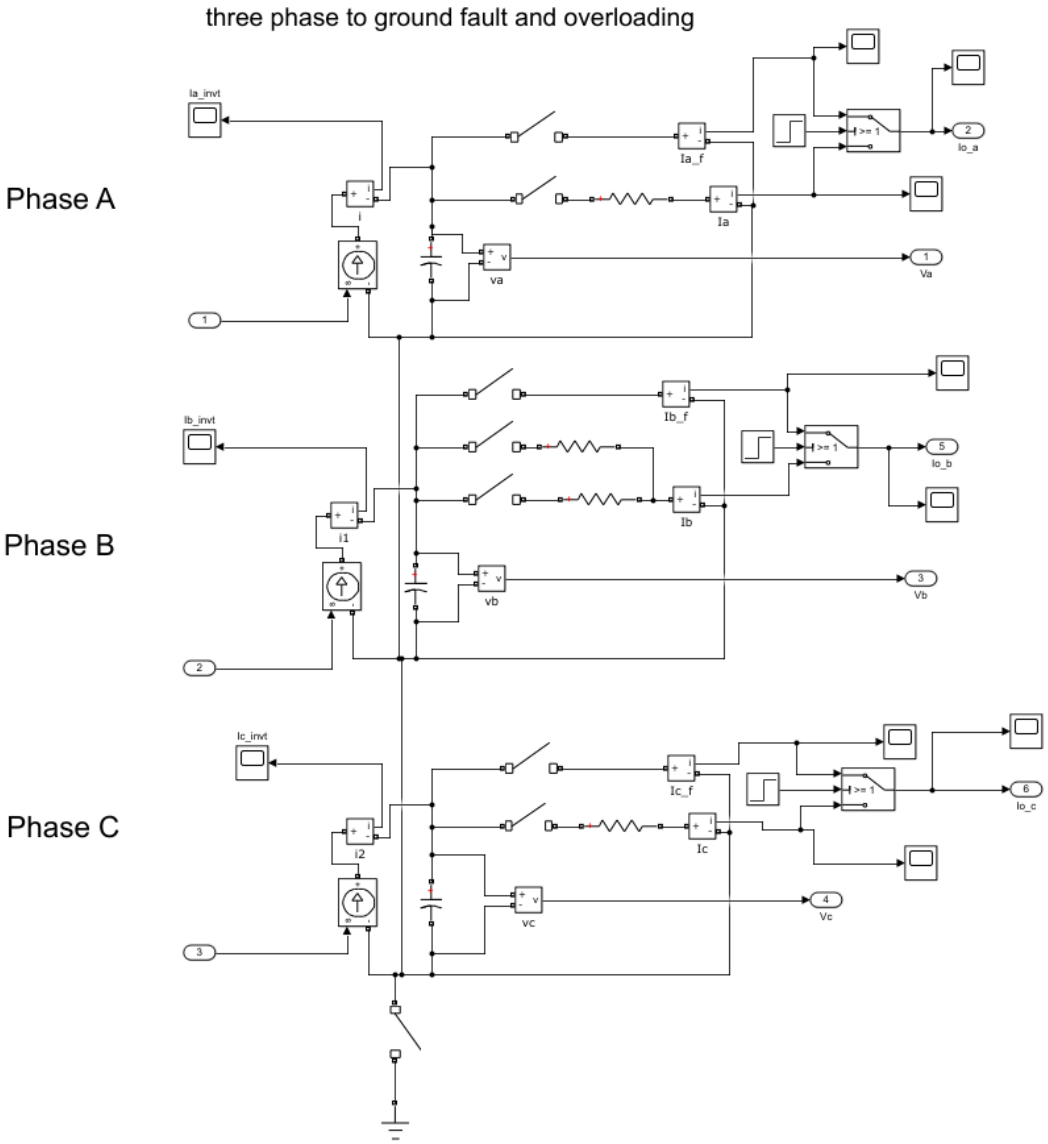
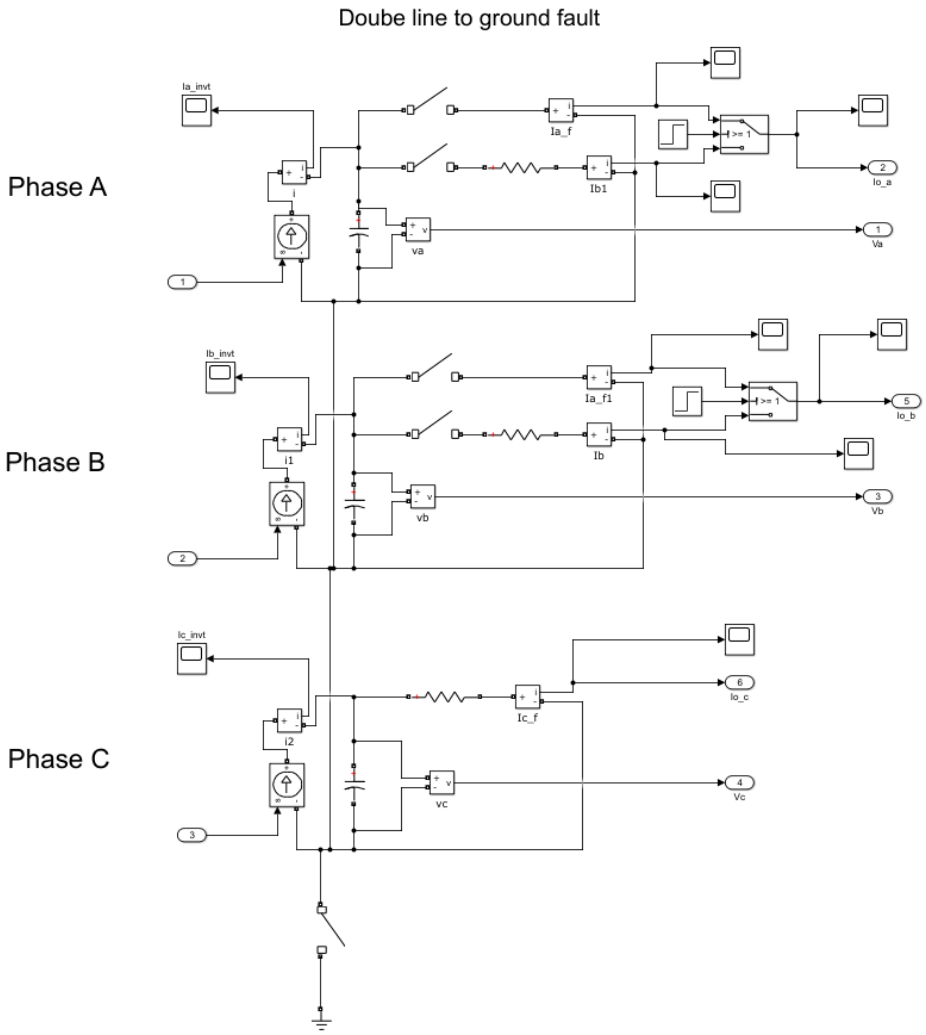

three phase to ground fault and overloading
Phase A
Phase B
Phase C
Ia_invt
Ib_invt
Ic_invt
Ia_f
Ib_f
Ic_f
Ia
Ib
Ic
va
vb
vc
Va
Vb
Vc
Io_a
Io_b
Io_c
i1
i2
>= 1

***Figure 5***




**Variable initialization**

```
close all
clc
clear all
%% Reference
U = 230.9; % V
f = 50; % Hz

%% Current limit
Ilim = 72; % A

%% Filter parameter
C1 = 5*6.8e-6;

%% Load impedance (resistive load)
R = (U)^2/(20e3/3); %20 kW load
P = 20e3/3;
Pf = 15e3;
```

# Appendix B : Overcurrent simulation results

This appendix contains the overcurrent laboratory test results of the 93PS unit. It consists of selected voltage and current waveforms for short circuit, ground faults and overloading. The short circuit tests were done using a provided black box to perform single line to ground, line to line, line to line to ground and three-phase to ground faults. Overloading was conducted according to the existing overload test guidelines for Eaton UPS units. Transformer inrush current was recorded during normal operation when the UPS system is loaded for the first time. The order and description of the figures is as listed below.

| Figure | Description |
|---|---|
| 1 | 93PS unfiltered single phase to ground fault in phase A |
| 2 | 93PS unfiltered double line fault in phases A and B |
| 3 | 93PS unfiltered double line to ground fault in phases A and B |
| 4 | 93PS unfiltered three-phase to ground fault |

***Figure 1***

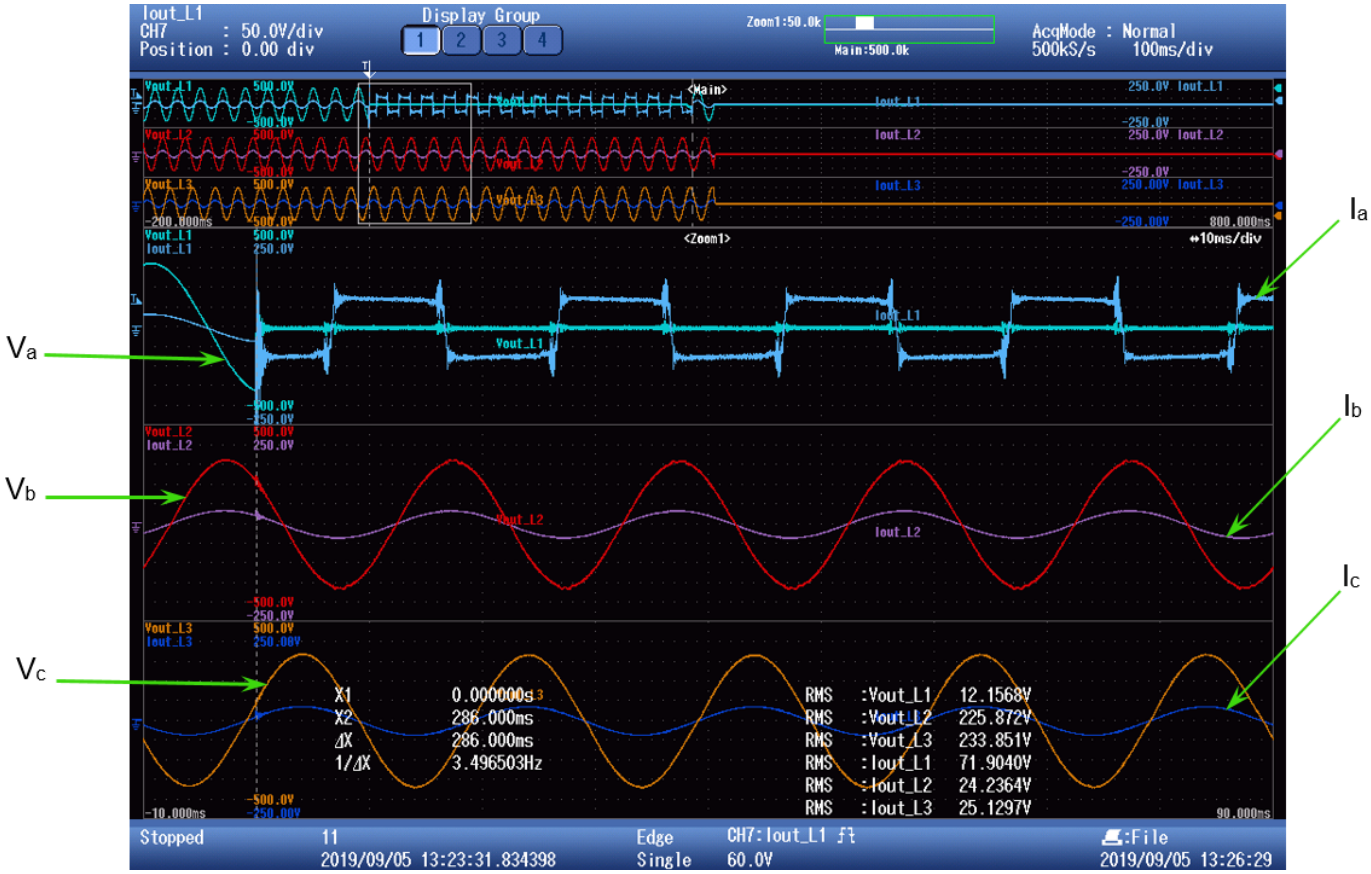


***Figure 2***

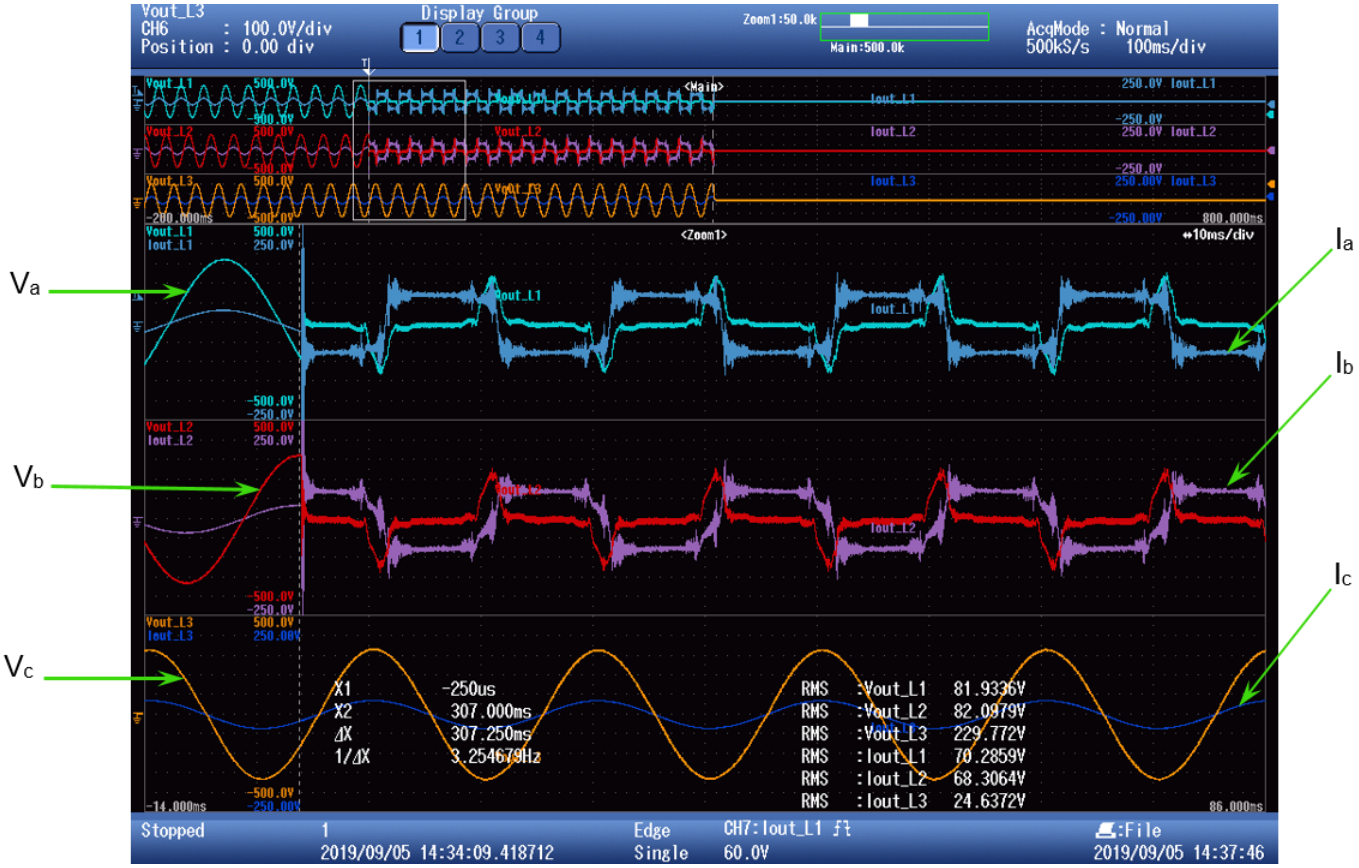

Va
Vb
Vc
Ia
Ib
Ic
Vout_L3
CH6 : 100.0V/div
Position : 0.00 div
Display Group
AcqMode : Normal
500kS/s 100ms/div
X1 -250us
X2 307.000ms
ΔX 307.250ms
1/ΔX 3.254679Hz
RMS :Vout_L1 81.9336V
RMS :Vout_L2 82.0979V
RMS :Vout_L3 229.772V
RMS :Iout_L1 70.2859V
RMS :Iout_L2 68.3064V
RMS :Iout_L3 24.6372V
Stopped
2019/09/05 14:34:09.418712
Edge
Single
CH7:Iout_L1
60.0V
2019/09/05 14:37:46

***Figure 3***


Va
Vb
Vc
Ia
Ib
Ic
Vout_L3
CH6 : 100.0V/div
Position : 0.00 div
Display Group
AcqMode : Normal
500kS/s 100ms/div
<Main>
<Zoom1>
X1 -250us
X2 305.900ms
ΔX 306.150ms
1/ΔX 3.266373Hz
RMS :Vout_L1 9.99316V
RMS :Vout_L2 9.72044V
RMS :Vout_L3 230.276V
RMS :Iout_L1 72.0156V
RMS :Iout_L2 72.0874V
RMS :Iout_L3 24.7265V
Stopped
2019/09/05 13:47:35.257741
Edge
Single
CH7:Iout_L1
60.0V
:File
2019/09/05 13:51:11

***Figure 4***


Va
Vb
Vc
Ia
Ib
Ic
Vout_L3
CH6 : 100.0V/div
Position : 0.00 div
Display Group
AcqMode : Normal
500kS/s 100ms/div
X1 -250us
X2 305.900ms
ΔX 306.150ms
1/ΔX 3.266373Hz
RMS :Vout_L1 8.07805V
RMS :Vout_L2 9.96215V
RMS :Vout_L3 6.71025V
RMS :Iout_L1 72.0721V
RMS :Iout_L2 72.5937V
RMS :Iout_L3 72.7064V
Stopped
2019/09/05 14:03:44.916116
Edge
Single
CH7:Iout_L1
60.0V
2019/09/05 14:05:07

# Appendix C : Overcurrent laboratory tests results

In this appendix, the overcurrent detection laboratory test results conducted on the 93PS unit running the detection algorithm of chapter 5 subsection 5.4, are presented. It consists of a detection signal indicating whether a fault has been detected and selected voltage and current waveforms for short circuits, ground fault and overloading. The order and description of the figures is as tabulated.

| Figure | Description |
|---|---|
| 1 | 93PS single phase to ground fault in phase A detected |
| 2 | 93PS single phase to ground faulted phase A waveform |
| 3 | 93PS single phase to ground fault healthy phases B and C waveforms |
| 4 | 93PS double line fault in phases A and B detected |
| 5 | 93PS double line faulted phase A waveform |
| 6 | 93PS double line faulted phase B waveform |
| 7 | 93PS double line fault healthy phase C waveform |
| 8 | 93PS double line to ground fault in phases A and B detected |
| 9 | 93PS double line to ground faulted phase A waveform |
| 10 | 93PS double line to ground faulted phase B waveform |
| 11 | 93PS double line to ground fault healthy phase C waveform |
| 12 | 93PS three-phase to ground fault in all phases detected |
| 13 | 93PS three-phase to ground faulted phase A waveform |
| 14 | 93PS three-phase to ground faulted phase B waveform |
| 15 | 93PS three-phase to ground faulted phase C waveform |
| 16 | Detection algorithm tested with 93PS $33kW$ overloading condition |

***Figure 1***


Iout_L3
CH9 : 50.00V/div
Position : 0.00 div
Display Group
1 2 3 4
Zoom1:25.0k
Main:500.0k
AcqMode : Normal
500kS/s 100ms/div
<Main>
<Zoom1>
+5ms/div
Vout_L1
Vout_L2
Vout_L3
Iout_L1
Iout_L2
Iout_L3
short_A
Short_B
Short_C
X1 0.000000s
X2 2.126ms
ΔX 2.126ms
1/ΔX 470.3669Hz
RMS :Vout_L1 8.68948V
RMS :Vout_L2 226.895V
RMS :Vout_L3 235.891V
RMS :Iout_L1 71.6840V
RMS :Iout_L2 16.3904V
RMS :Iout_L3 17.0607V
Stopped
1
2019/10/04 15:11:49.063655
Edge
Single
CH7:Iout_L1
62.0V
:File
2019/10/04 15:13:46

***Figure 2***


detector
$V_a$
$I_a$
Vout_L1
CH4 : 100.0V/div
Position : 0.00 div
Display Group
1 2 3 4
Zoom1:25.0k
Main:500.0k
AcqMode : Normal
500kS/s 100ms/div
<Main>
short_A
<Zoom1>
+5ms/div
X1 0.000000s
X2 2.126ms
ΔX 2.126ms
1/ΔX 470.3669Hz
RMS :Vout_L1 8.68948V
RMS :Iout_L1 71.6840V
Stopped
2019/10/04 15:11:49.063655
Edge
Single
CH7:Iout_L1 62.0V
:File
2019/10/04 15:14:59

***Figure 3***

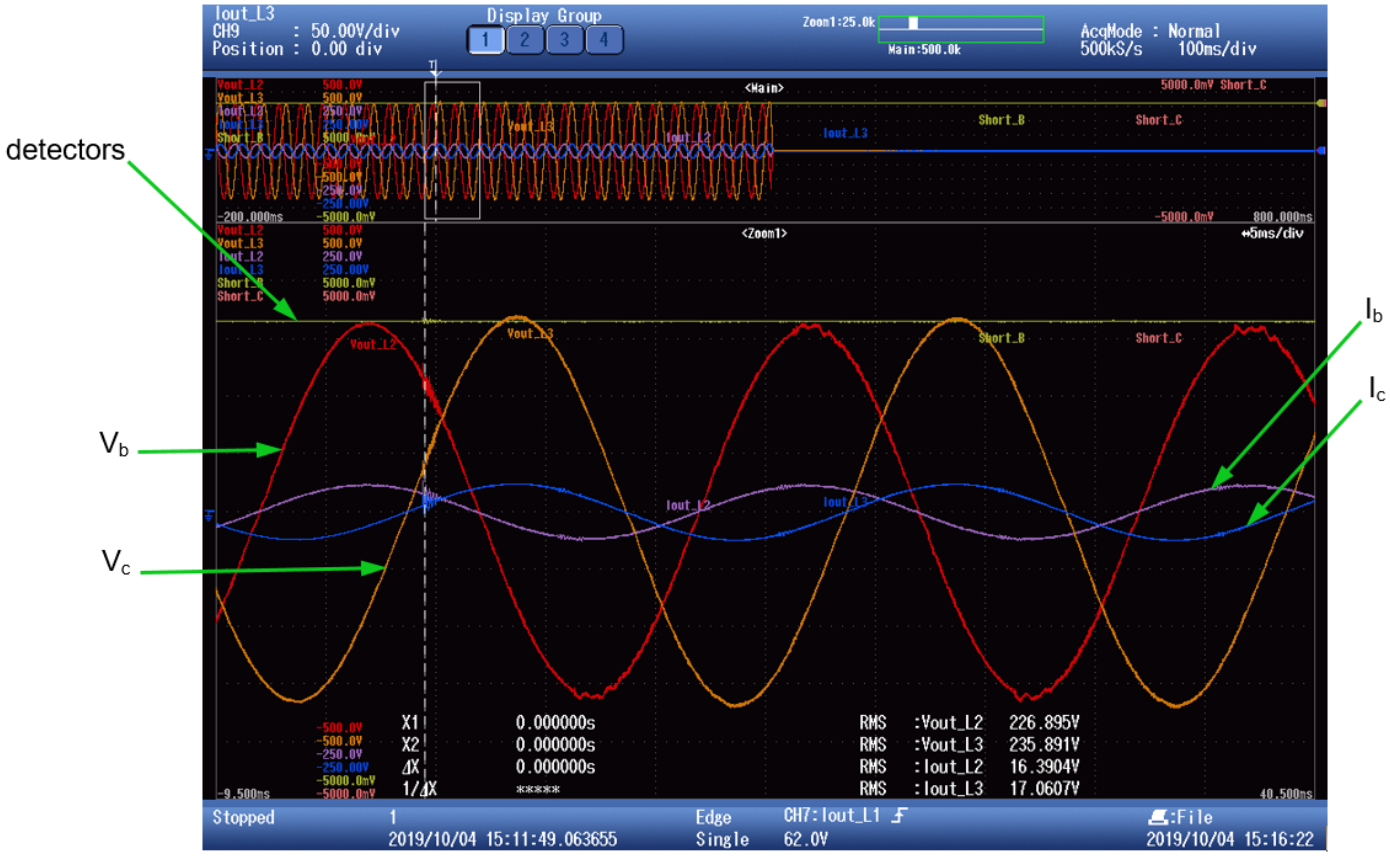

detectors
$V_b$
$V_c$
$I_b$
$I_c$
Iout_L3
CH9 : 50.00V/div
Position : 0.00 div
Display Group
1 2 3 4
Zoom1:25.0k
Main:500.0k
AcqMode : Normal
500kS/s 100ms/div
<Main>
<Zoom1>
Vout_L2
Vout_L3
Iout_L2
Iout_L3
Short_B
Short_C
X1 0.000000s
X2 0.000000s
ΔX 0.000000s
1/ΔX *****
RMS :Vout_L2 226.895V
RMS :Vout_L3 235.891V
RMS :Iout_L2 16.3904V
RMS :Iout_L3 17.0607V
Stopped
2019/10/04 15:11:49.063655
Edge
Single
CH7:Iout_L1
62.0V
:File
2019/10/04 15:16:22

***Figure 4***


Vout_L3
CH6 : 100.0V/div
Position : 0.00 div
Display Group
1 2 3 4
Zoom1:25.0k
Main:500.0k
AcqMode : Normal
500kS/s 100ms/div
<Main>
<Zoom1>
+5ms/div
Vout_L1
Vout_L2
Vout_L3
Iout_L1
Iout_L2
Iout_L3
short_A
Short_B
Short_C
X1 0.000000s
X2 13.100ms
ΔX 13.100ms
1/ΔX 76.33588Hz
RMS :Vout_L1 83.1856V
RMS :Vout_L2 83.5477V
RMS :Vout_L3 231.534V
RMS :Iout_L1 70.3571V
RMS :Iout_L2 69.0732V
RMS :Iout_L3 16.7353V
Stopped
2019/10/04 14:42:22.079162
Edge
Single
CH8:Iout_L2
66.0V
:File
2019/10/04 14:43:22

***Figure 5***


detector
$V_a$
$I_a$
Vout_L1
CH4 : 100.0V/div
Position : 0.00 div
Display Group
1 2 3 4
Zoom1:25.0k
Main:500.0k
AcqMode : Normal
500kS/s 100ms/div
<Main>
short_A
<Zoom1>
+5ms/div
X1 0.000000s
X2 5.326ms
ΔX 5.326ms
1/ΔX 187.7582Hz
RMS :Vout_L1 83.4652V
RMS :Iout_L1 70.3702V
Stopped
2019/10/04 14:44:37.949762
Edge
Single
CH8:Iout_L2
66.0V
:File
2019/10/04 14:47:18

***Figure 6***


detector
Vb
Ib
Short_B
CH11 : 1.0000V/div
Position : 0.00 div
Display Group
1 2 3 4
Zoom1:25.0k
Main:500.0k
AcqMode : Normal
500kS/s 100ms/div
Vout_L2 500.0V
Iout_L2 250.0V
Short_B 5000.0mV
<Main>
-200.000ms
800.000ms
<Zoom1>
↔5ms/div
X1 0.000000s
X2 15.200ms
ΔX 15.200ms
1/ΔX 65.78947Hz
RMS :Vout_L2 83.7905V
RMS :Iout_L2 69.0699V
-9.500ms
40.500ms
Stopped
1
2019/10/04 14:44:37.949762
Edge
Single
CH8:Iout_L2
66.0V
:File
2019/10/04 14:48:17

***Figure 7***

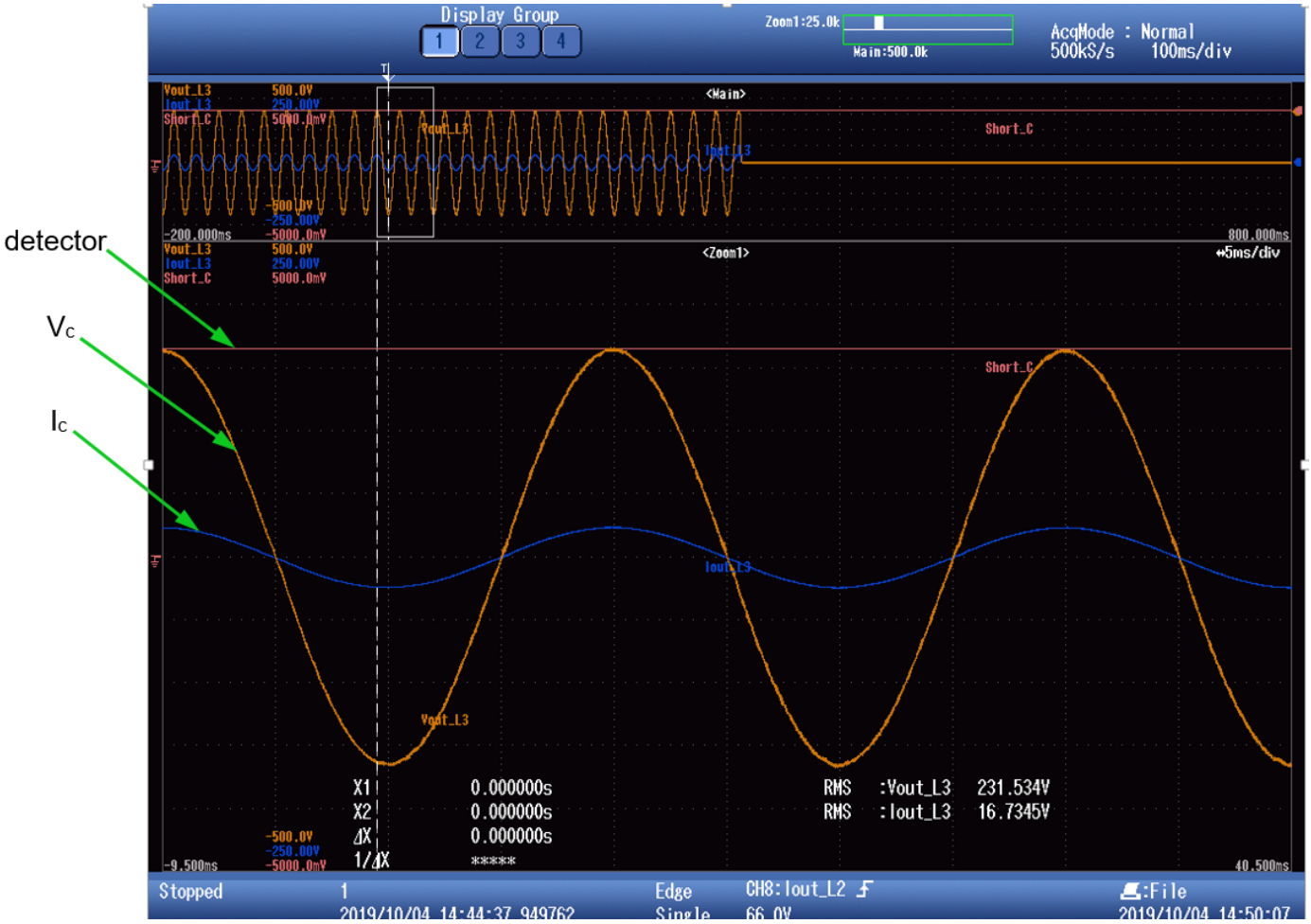

detector
Vc
Ic
Display Group
1 2 3 4
Zoom1:25.0k
Main:500.0k
AcqMode : Normal
500kS/s 100ms/div
Vout_L3 500.0V
Iout_L3 250.00V
Short_C 5000.0mV
<Main>
Short_C
Iout_L3
-200.000ms
800.000ms
<Zoom1>
+5ms/div
X1 0.000000s
X2 0.000000s
ΔX 0.000000s
1/ΔX *****
RMS :Vout_L3 231.534V
RMS :Iout_L3 16.7345V
-9.500ms
40.500ms
Stopped
Edge
CH8:Iout_L2
:File

***Figure 8***


Vout_L3
CH6 : 100.0V/div
Position : 0.00 div
Display Group
1 2 3 4
Zoom1:25.0k
Main:500.0k
AcqMode : Normal
500kS/s 100ms/div
<Main>
<Zoom1>
+5ms/div
X1 0.000000s
X2 2.826ms
ΔX 2.826ms
1/ΔX 353.8570Hz
Max :short_A 3310.0mV
Min :short_A 3.8mV
RMS :Vout_L1 8.13681V
RMS :Vout_L3 231.871V
RMS :Iout_L1 72.2271V
RMS :Iout_L2 72.2151V
RMS :Iout_L3 16.7812V
RMS :short_A 321.674mV
RMS :Short_B 313.527mV
RMS :Short_C 3.31258V
Stopped
6
2019/10/04 13:19:53.117642
Edge
Single
CH8:Iout_L2
66.0V
:File
2019/10/04 13:21:49

***Figure 9***


detector
$I_a$
Display Group
1 2 3 4
Zoom1:25.0k
Main:500.0k
AcqMode : Normal
500kS/s 100ms/div
Iout_L1 250.0V
short_A 5000.0mV
<Main>
short_A
Iout_L1
-200.000ms
800.000ms
<Zoom1>
•5ms/div
X1 0.000000s
X2 2.826ms
ΔX 2.826ms
1/ΔX 353.8570Hz
Max :short_A 3310.0mV
Min :short_A 3.8mV
RMS :Iout_L1 72.2271V
RMS :short_A 321.674mV
-8.500ms
41.500ms
Stopped
6
2019/10/04 13:19:53.117642
Edge
Single
CH8: Iout_L2
66.0V
:File
2019/10/04 13:22:42

***Figure 10***


detector
Vb
Ib
Iout_L2
CH8 : 50.0V/div
Position : 0.00 div
Display Group
1 2 3 4
Zoom1:25.0k
Main:500.0k
AcqMode : Normal
500kS/s 100ms/div
<Main>
Short_B
<Zoom1>
X1 0.000000s
X2 2.526ms
ΔX 2.526ms
1/ΔX 395.8828Hz
RMS :Vout_L2 10.6704V
RMS :Iout_L2 72.2151V
RMS :Short_B 313.527mV
Stopped
2019/10/04 13:19:53.117642
Edge
Single
CH8:Iout_L2
66.0V
:File
2019/10/04 13:41:25

***Figure 11***


detector
$V_c$
$I_c$
Iout_L3
CH9 : 50.00V/div
Position : 0.00 div
Display Group
1 2 3 4
Zoom1:25.0k
Main:500.0k
AcqMode : Normal
500kS/s 100ms/div
<Main>
Short_C
Vout_L3
Iout_L3
<Zoom1>
+5ms/div
X1 0.000000s
X2 0.000000s
ΔX 0.000000s
1/ΔX *****
RMS :Vout_L3 231.871V
RMS :Iout_L3 16.7812V
RMS :Short_C 3.31258V
Stopped
6
2019/10/04 13:19:53.117642
Edge
Single
CH8:Iout_L2
66.0V
:File
2019/10/04 13:40:33

***Figure 12***


detectors
$I_a$
$I_b$
$I_c$
Iout_L3
CH9 : 50.00V/div
Position : 0.00 div
Display Group
1 2 3 4
Zoom1:25.0k
Main:500.0k
AcqMode : Normal
500kS/s 100ms/div
<Main>
<Zoom1>
Iout_L1
Iout_L2
Iout_L3
short_A
Short_B
Short_C
X1 -150us
X2 5.900ms
ΔX 6.050ms
1/ΔX 165.2893Hz
Max :short_A 3310.4mV
Min :short_A 3.3mV
RMS :Iout_L1 71.4266V
RMS :Iout_L2 71.8328V
RMS :Iout_L3 72.2855V
RMS :short_A 517.082mV
RMS :Short_B 430.267mV
RMS :Short_C 411.885mV
Stopped
4
2019/10/04 12:45:17.361246
Edge
Single
CH8:Iout_L2
66.0V
:File
2019/10/04 12:46:17

***Figure 13***


detector
$I_a$
Display Group
1
2
3
4
Zoom1:25.0k
Main:500.0k
AcqMode : Normal
500kS/s
100ms/div
Iout_L1 250.0V
short_A 5000.0mV
<Main>
short_A
-200.000ms
800.000ms
<Zoom1>
+5ms/div
Iout_L1
short_A
X1 -150us
X2 5.150ms
ΔX 5.300ms
1/ΔX 188.6792Hz
Max :short_A 3310.0mV
Min :short_A 3.3mV
RMS :Iout_L1 72.1003V
RMS :short_A 433.056mV
-12.500ms
37.500ms
Stopped
4
2019/10/04 12:45:17.361246
Edge
Single
CH8:Iout_L2
66.0V
:File
2019/10/04 12:48:20

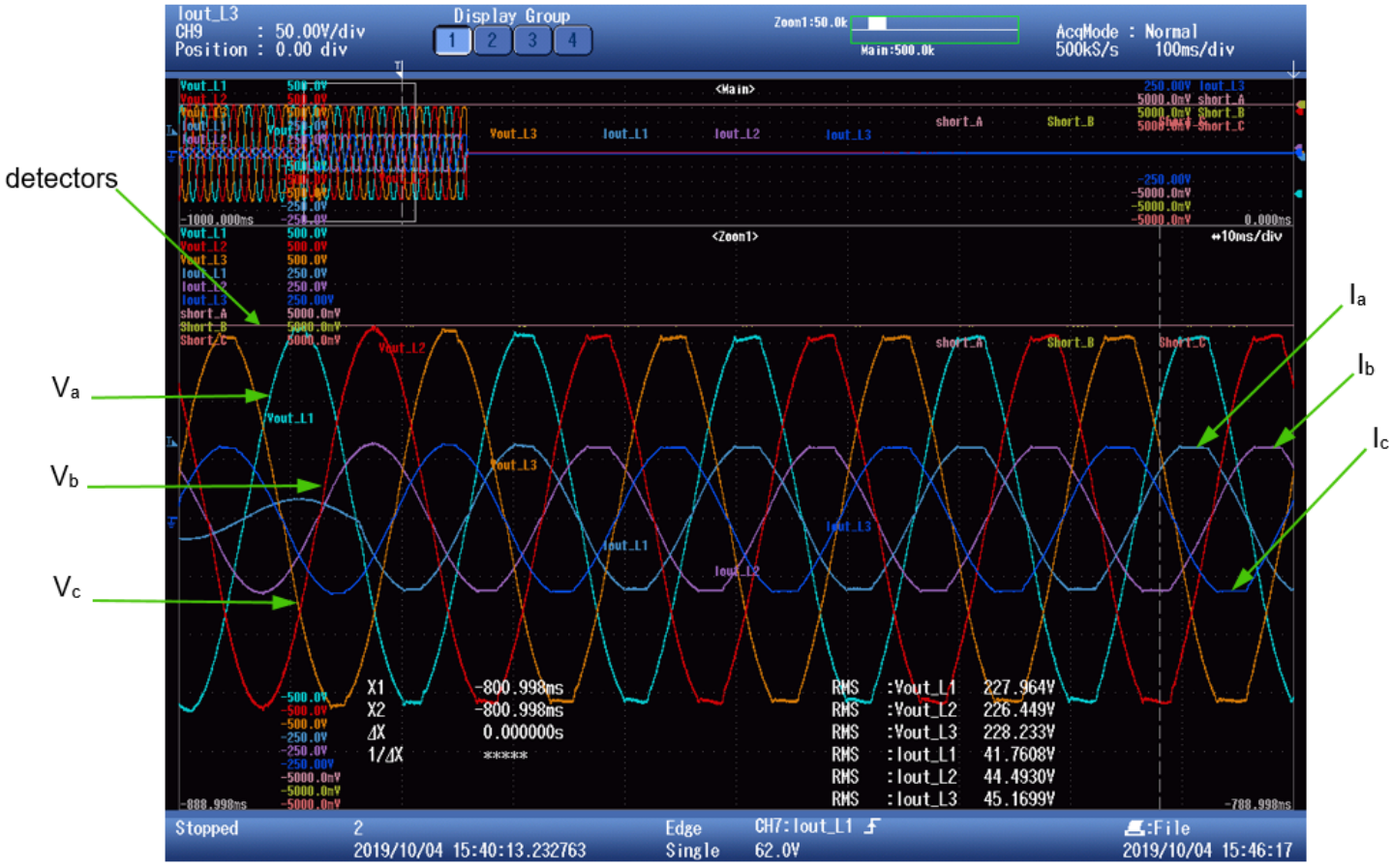
***Figure 14***


detector
Ib
Short_B
CH11 : 1.0000V/div
Position : 0.00 div
Display Group
1 2 3 4
Zoom1:25.0k
Main:500.0k
AcqMode : Normal
500kS/s 100ms/div
Iout_L2 250.0V
Short_B 5000.0mV
<Main>
-200.000ms
800.000ms
<Zoom1>
+5ms/div
X1 -150us
X2 2.926ms
ΔX 3.076ms
1/ΔX 325.0975Hz
RMS :Iout_L2 72.5140V
RMS :Short_B 332.776mV
-12.500ms
37.500ms
Stopped
4
2019/10/04 12:45:17.361246
Edge
Single
CH8:Iout_L2
66.0V
:File
2019/10/04 12:49:10

***Figure 15***


detector
$I_C$
Short_C
CH12 : 1.0000V/div
Position : 0.00 div
Display Group
Zoom1:25.0k
Main:500.0k
AcqMode : Normal
500kS/s 100ms/div
Iout_L3 250.00V
Short_C 5000.0mV
<Main>
Short_C
-200.000ms
800.000ms
<Zoom1>
•5ms/div
X1 -150us
X2 2.226ms
ΔX 2.376ms
1/ΔX 420.8754Hz
RMS :Iout_L3 72.9663V
RMS :Short_C 293.938mV
-12.500ms
37.500ms
Stopped
4
2019/10/04 12:45:17.361246
Edge
Single
CH8:Iout_L2
66.0V
:File
2019/10/04 12:49:58

***Figure 16***


detectors
Va
Vb
Vc
Ia
Ib
Ic
Iout_L3
CH9 : 50.00V/div
Position : 0.00 div
Display Group
1 2 3 4
Zoom1:50.0k
Main:500.0k
AcqMode : Normal
500kS/s 100ms/div
<Main>
<Zoom1>
↔10ms/div
X1 -800.998ms
X2 -800.998ms
ΔX 0.000000s
1/ΔX *****
RMS :Vout_L1 227.964V
RMS :Vout_L2 226.449V
RMS :Vout_L3 228.233V
RMS :Iout_L1 41.7608V
RMS :Iout_L2 44.4930V
RMS :Iout_L3 45.1699V
Stopped
2019/10/04 15:40:13.232763
Edge
Single
CH7:Iout_L1
62.0V
:File
2019/10/04 15:46:17